Перспективные туннельные транзисторы для интегральных схем сверхнизкого энергопотребления

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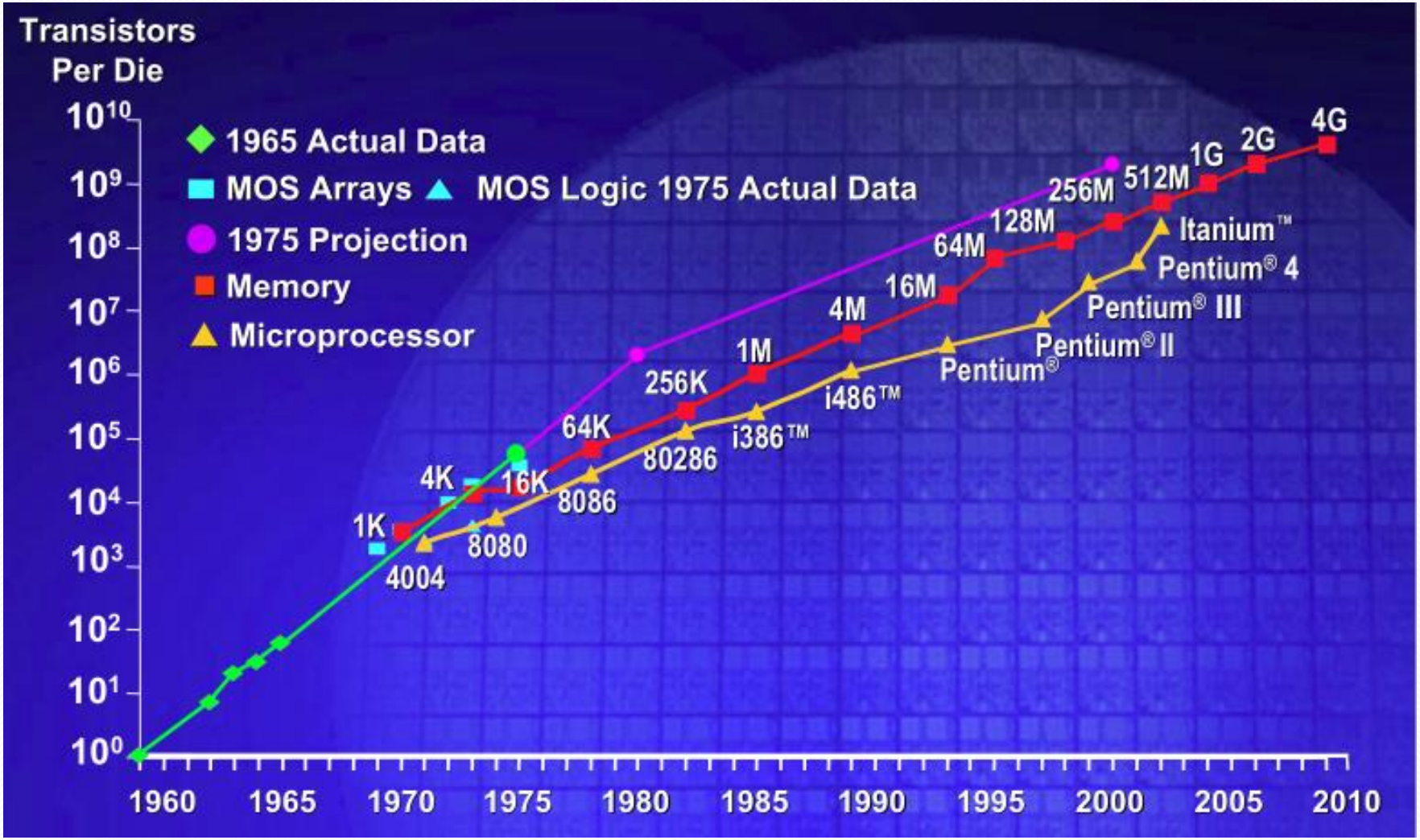
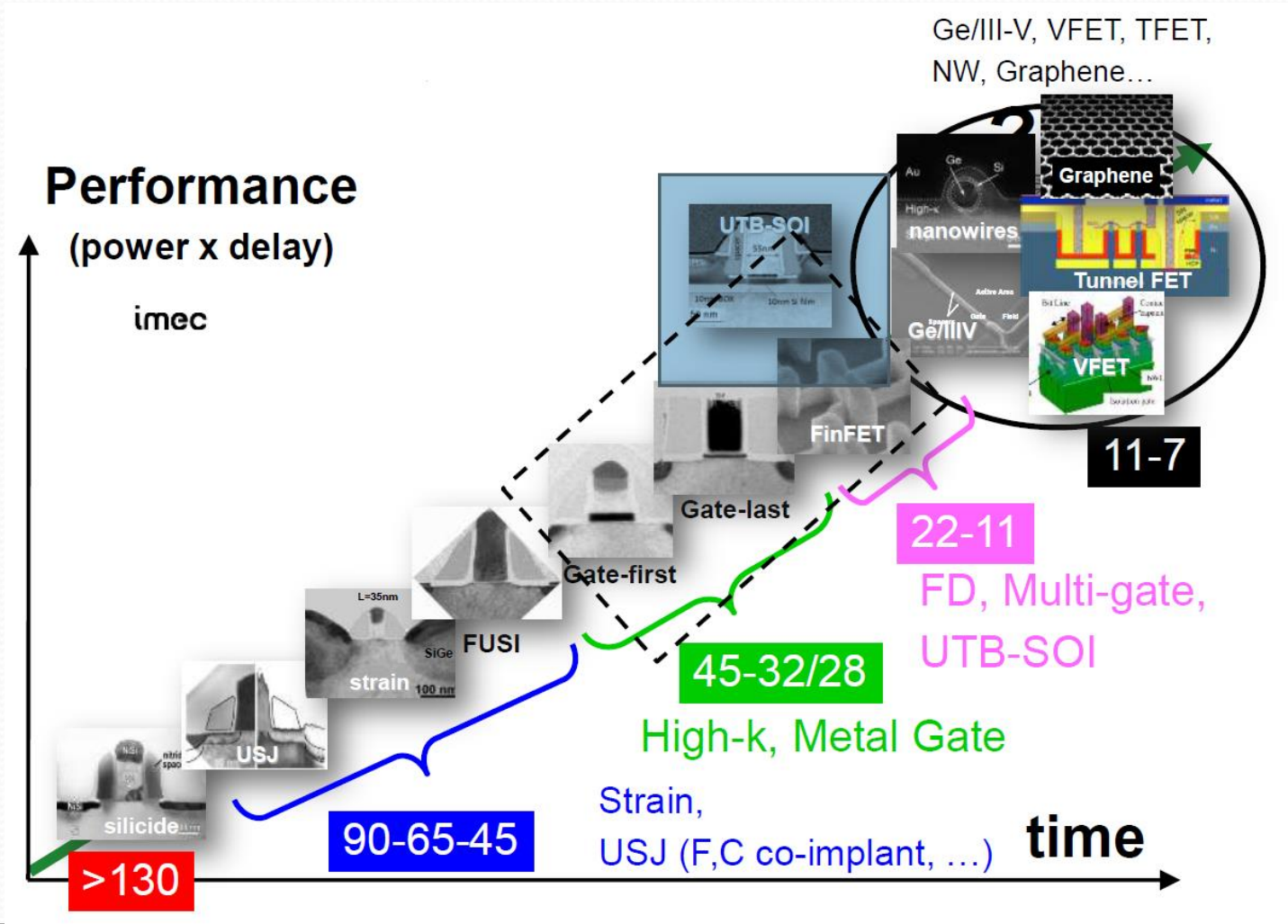
План

- Квантовые методы моделирования finFET.
- Туннельные транзисторы:
- увеличение крутизны => снижение рабочего напряжения => уменьшение разогрева => увеличение тактовой частоты.
- Полевые транзисторы на основе графена.

The end of Moore's 'law'?

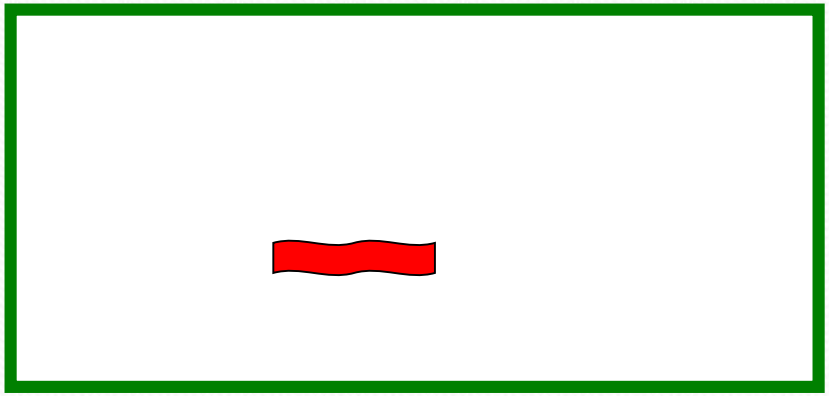


Технологии перспективных наноструктур CD<10 нм



SIMULATION

Where does nanoelectronics start from?



Micrometer channel length

Nanometer channel length

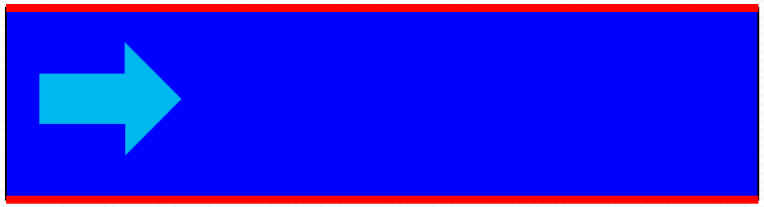
Semiconductors $\lambda_T \approx 10\ \text{nm}$

Metals $\lambda_F \approx 1\ \text{nm}$

Evolution of models

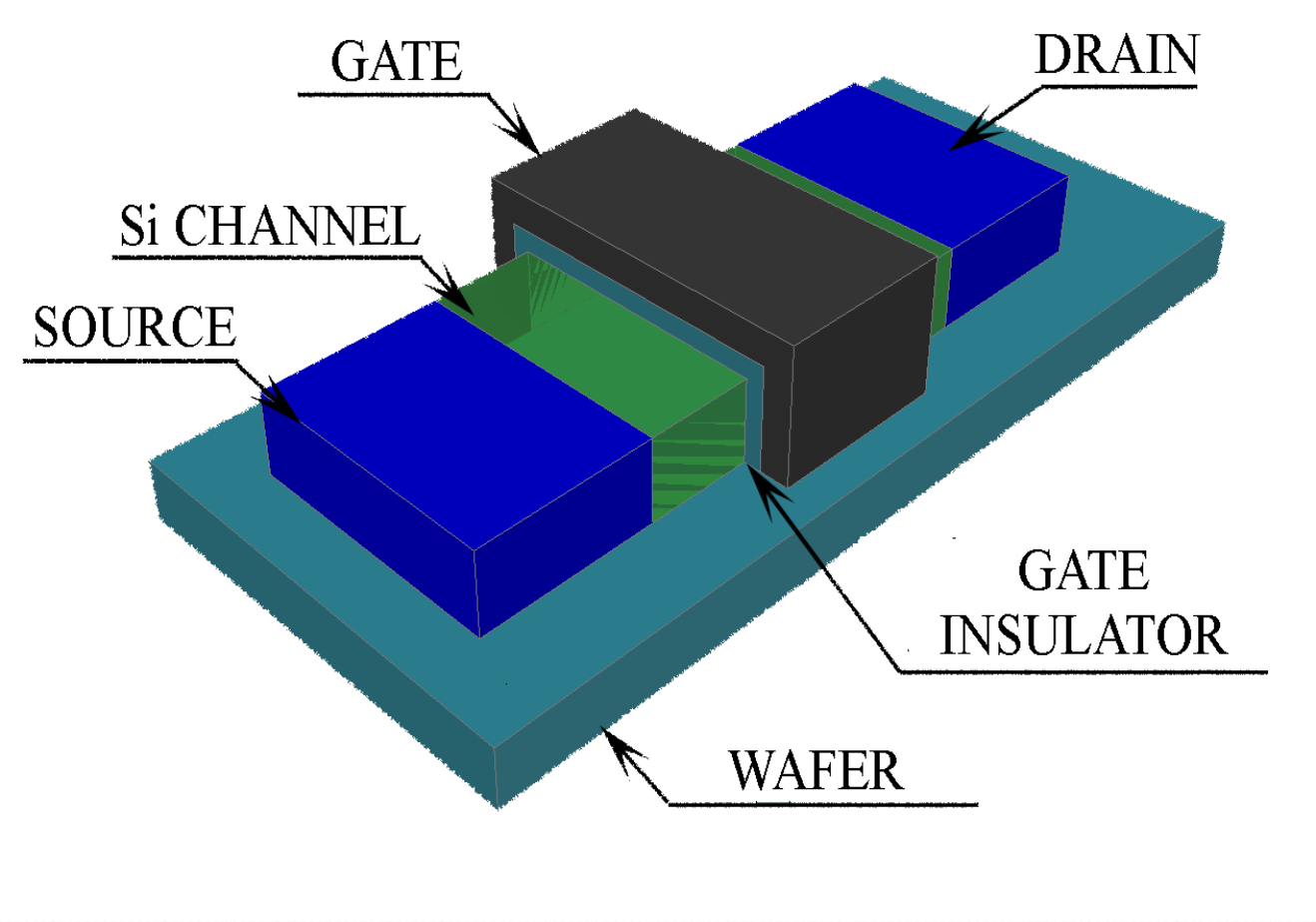
Charged waves:
Schrödinger equation

Charged particles:
Boltzmann kinetic equation



Charged fluid:
Hydrodynamic equations

Structure in simulation



Quantum effects in nanotransistors

- Fermi-Dirac statistics.
- Transversal quantization in channel:
- Quantum longitudinal motion:
  a) interference on random impurities;
  b) quantum reflection;
  c) source-drain tunneling.

Main strategy of simulation

- Self-consistent solution of

Schrödinger equation

+

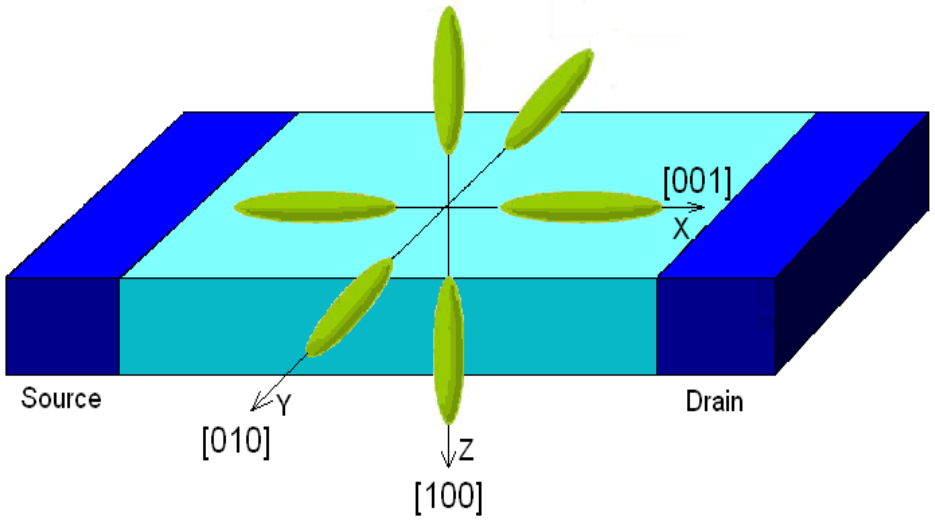
Maxwell equation

(Poisson equation)

Silicon conduction band structure

- Effective mass and transversal quantization energy

$$m_t = 0.19m_0, m_l = 0.98m_0$$



$$\varepsilon_0 = \frac{\hbar^2}{2m}\left[\frac{\pi}{d_{Si}}\right]^2$$

Quantum description

Charged waves:
Schrödinger equation

- Transversal quantization
- Wave-guide modes in the channel
- Landauer-Buttiker formalism

$$I(V_{sd}) = \frac{2e}{h}\sum_{i=0}^{\infty}\int dE T_i(E)\left[f_s(E) - f_d(E)\right]$$

Solution of 3D Schrödinger equation

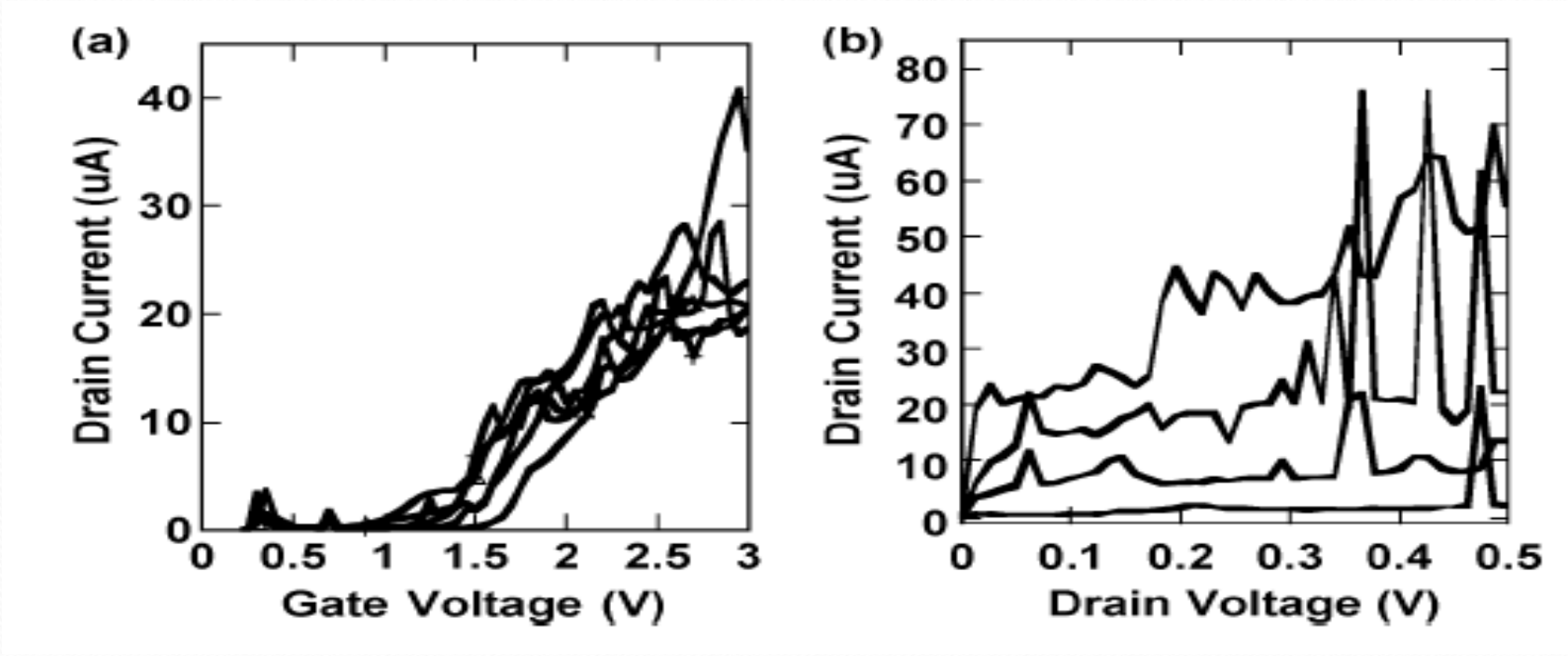
- $$-\frac{\hbar^2}{2m}\Delta\Psi(x,y,z)+V(x,y,z)\Psi(x,y,z)=\varepsilon\Psi(x,y,z)$$

  V(x,y,z) is a potential.

The direct solution of the stationary 3D Schrödinger equation via a finite difference scheme comes across a well known instability caused by **evanescent modes.**

In fact, the exponential growth of upper modes makes a **computation impossible**.

D.K.Ferry et al. (2005) (США, Arizona State University): results of simulation



Solution of Schrödinger equation:

transverse mode representation + high-precision arithmetic

$$\Psi(x,y,z) = \sum_{i=1}^{N} a_i(x)\psi_i(y,z)$$

where ψi(y,z) is the i-th transverse mode wave function,
N is a number of involved modes.

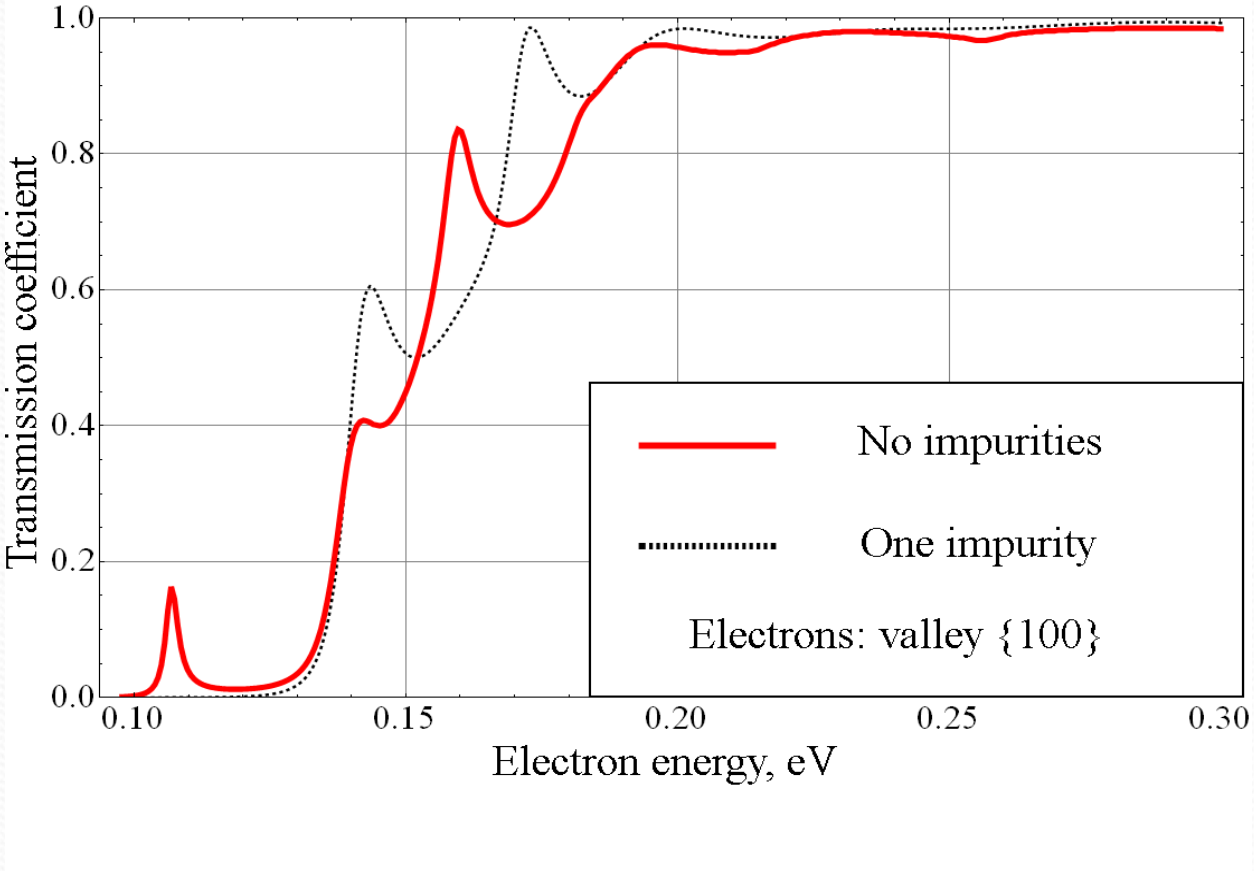
The space evolution of coefficients $a_i(x)$ is governed by matrix elements

$$M_{ij}(x) = <\psi_i(y,z)|V(x,y,z)|\psi_j(y,z)>$$

The off-diagonal elements M_{ij} manage the mode conversion.

The diagonal elements M_{ii} manage the quantum reflection, interference and tunneling of the i-th mode.

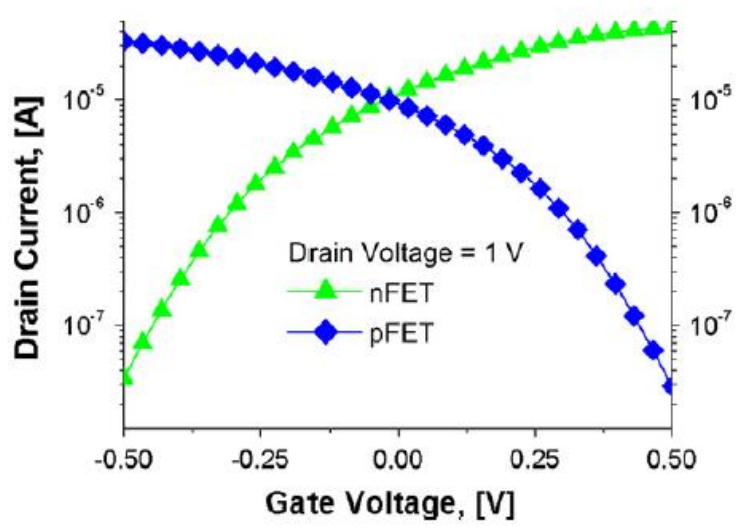
Calculated transmission coefficient vs. electron energy E

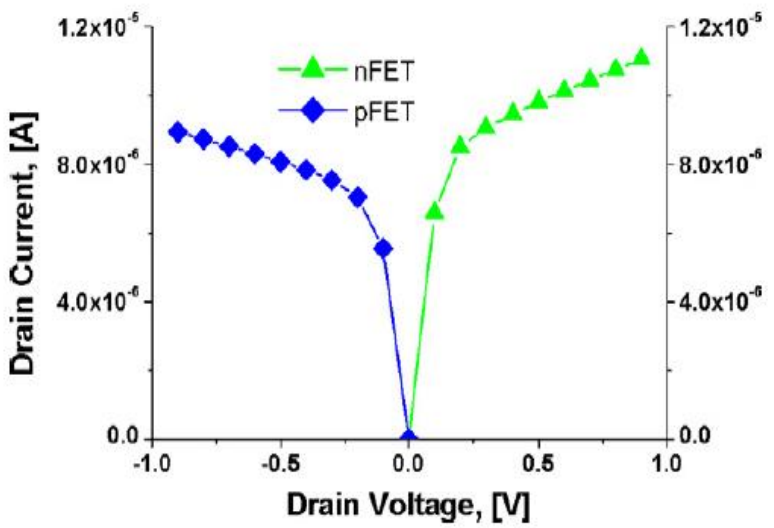


Transistor parameters are 10nm channel length and width, 5nm body thickness, 10^20 cm^-3 source/drain contact doping, 5nm spacers.

Quantum simulation of UTB FD MOSFET

10 nm gate length and 3 nm silicon body thickness

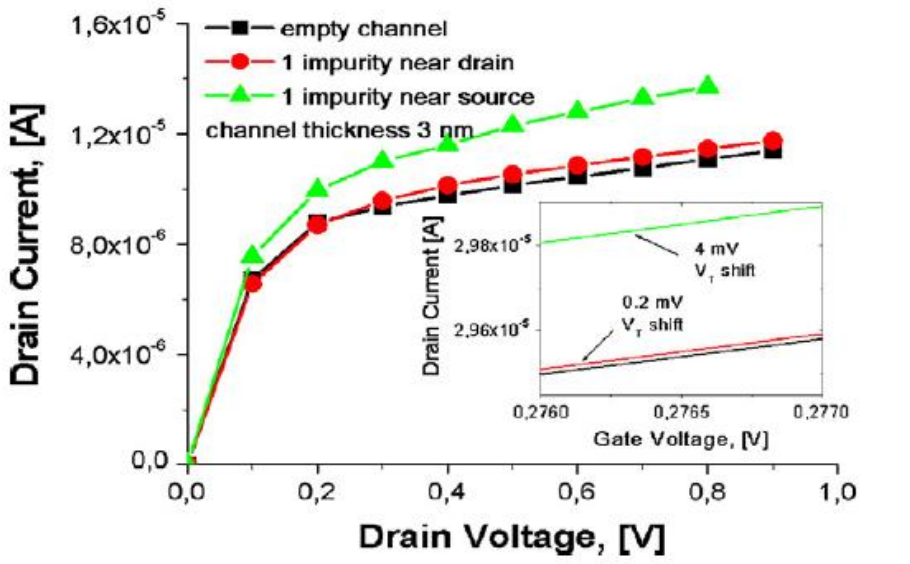




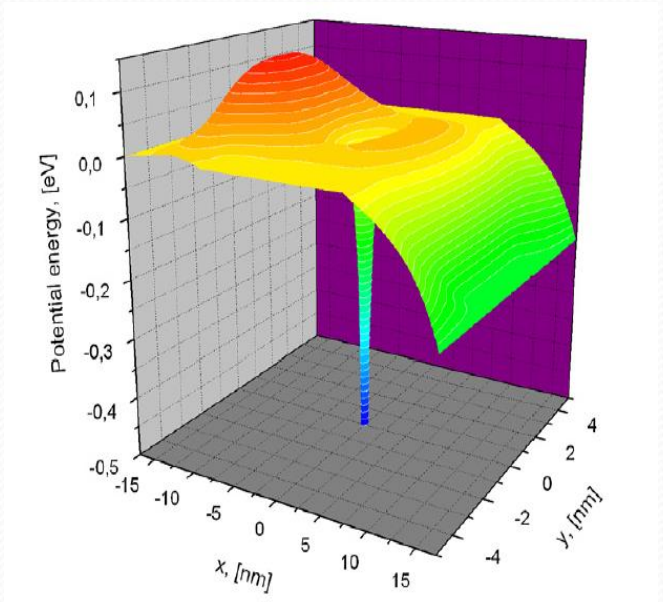
V. Vyurkov et al. Solid State Electronics. 2012.

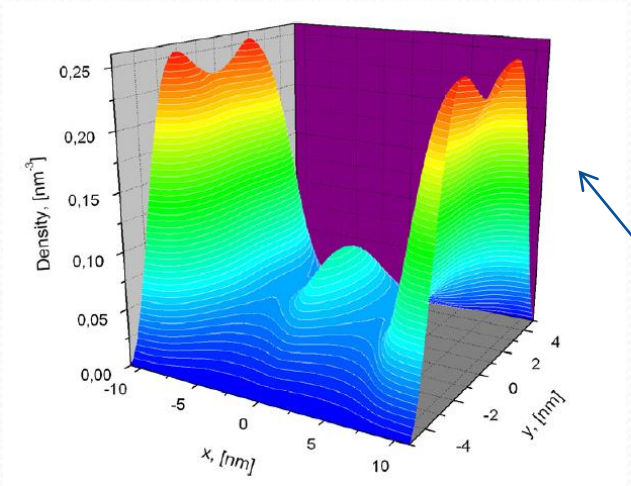
ФТИАН

Random charged centers in channel



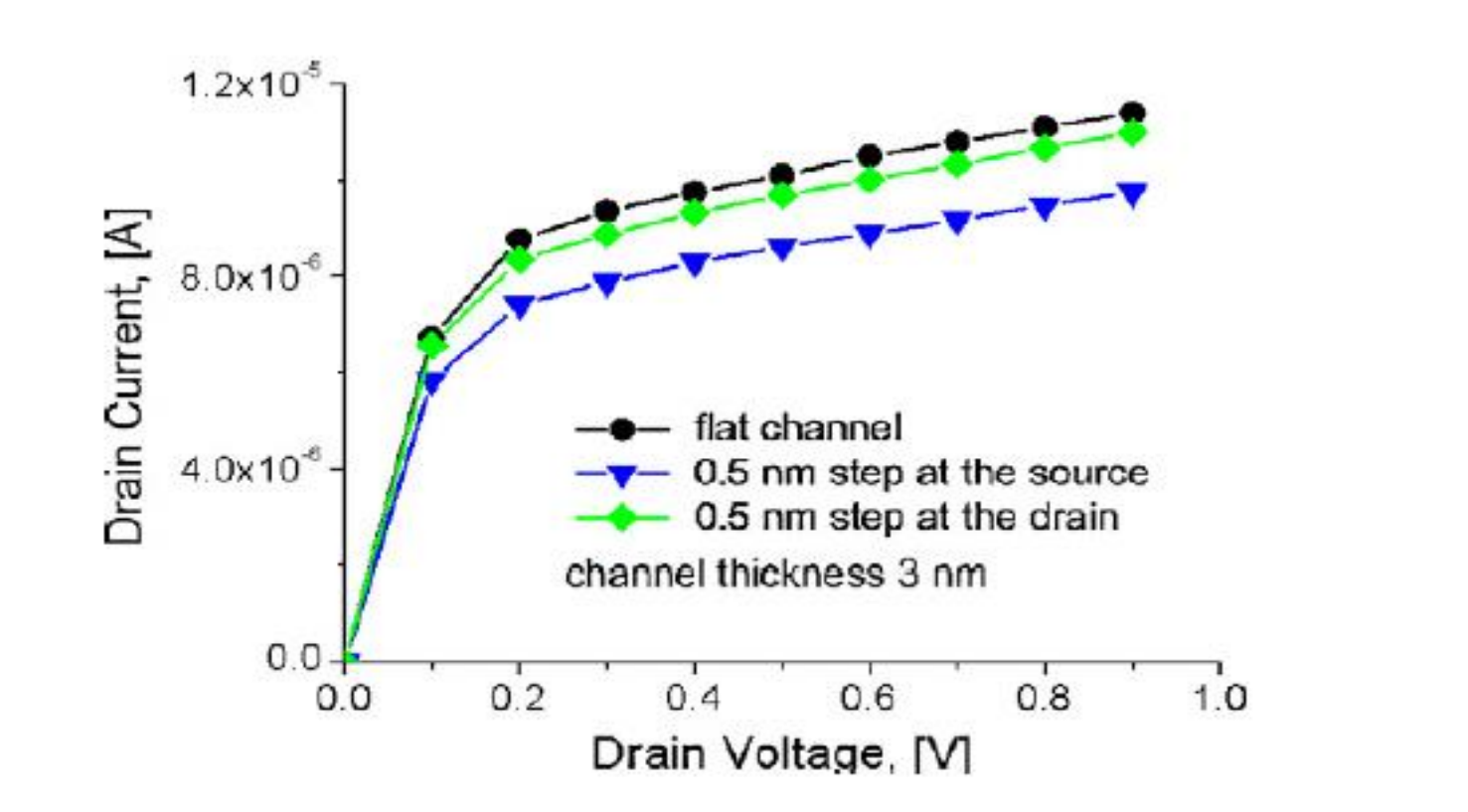
Two-dimensional self-consistent potential energy relief in the channel





Two-dimensional distribution of electron density in the channel

Wall roughness



ФТИАН

Dispersion of characteristics

- 5-15% in calculated I-V curves
- < 10% is an everlasting condition for large integrated circuits
- More severe demands to technology may arise.

Classical vs. quantum: quantum noise

Classical Schottky's shot noise
(spectral density of white noise at arbitrary temperature)

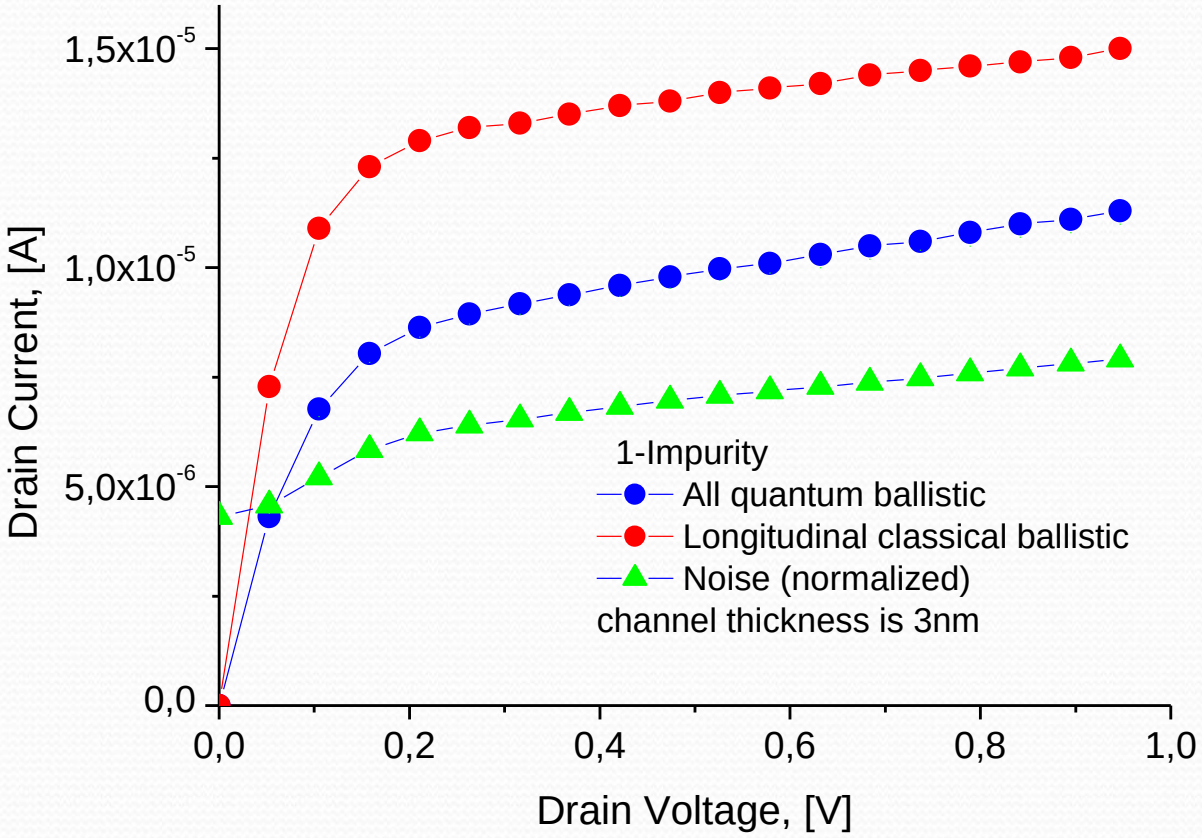
$$S(f)=2e|I|$$

G. B. Lesovik. Quantum excess noise in two-dimensional ballistic microcontacts. JETP Lett. 49 (1989) 594 (**zero temperature** T=0, Fermi-Dirac statistics)

$$dI_n^2 = \frac{2e^2}{h}\Delta\nu\,|eV|\,T(E)(1-T(E))$$

V. Vyurkov et al. Solid State Electronics. 2012
Quantum measurement theory to calculate the quantum noise at **finite temperature**

Quantum noise in simulated FETs



- Требования к современной электронике

Требования к современной электронике: 1) high performance

- RC задержка инвертора
- delay time = Rin * Cout
- Необходима высокая проводимость канала транзисторов и малый размер транзистора

- Предельная частота:
- пролётное время

$$f_{\max} = \frac{v}{L_{ch}}$$

- Необходима малая длина канала (Intel – 22nm)
- и/или высокая подвижность (новые материалы)

Требования к современной электронике: 2) low power

- Потребляемая **активная мощность**

$$P_a = \frac{CV_{DD}^2}{2} f$$

- Необходимо малое напряжение питания и быстрое переключение между состояниями

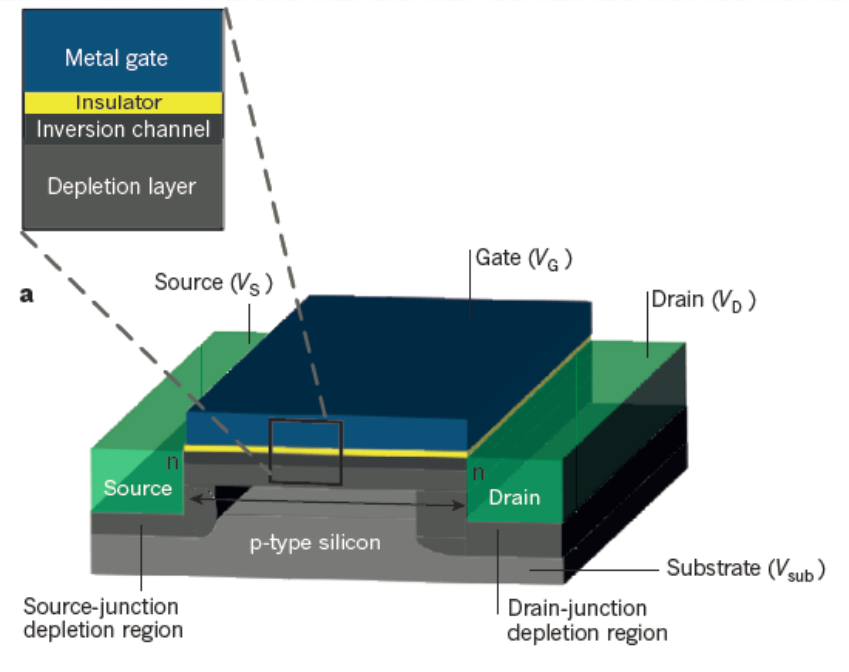
- **Пассивная мощность**

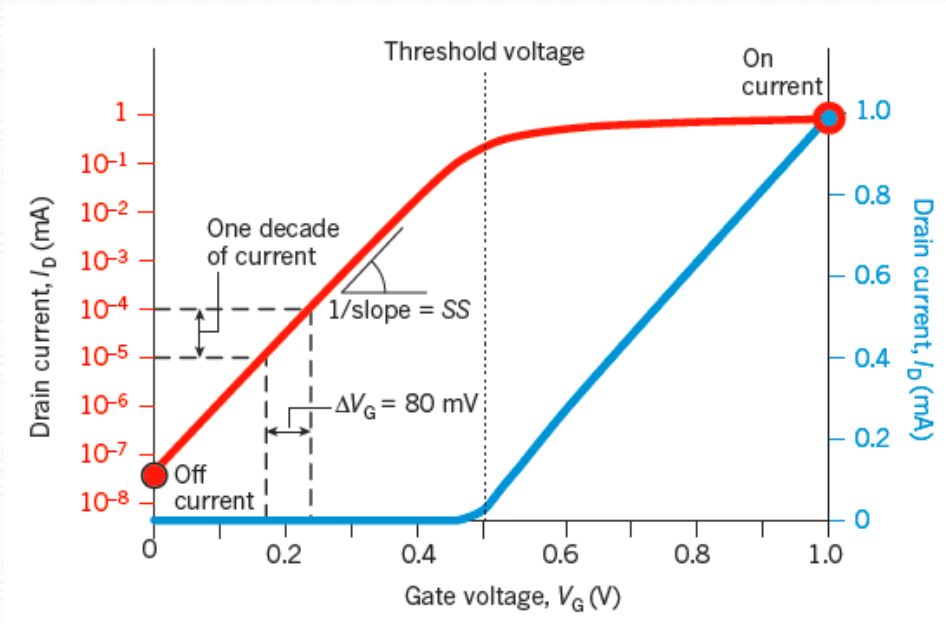
$$P_p = I_{OFF} V_{DD}$$

- Необходим малый ток в закрытом состоянии
- Большое отношение

$$I_{ON} / I_{OFF}$$

Снижение энергопотребления





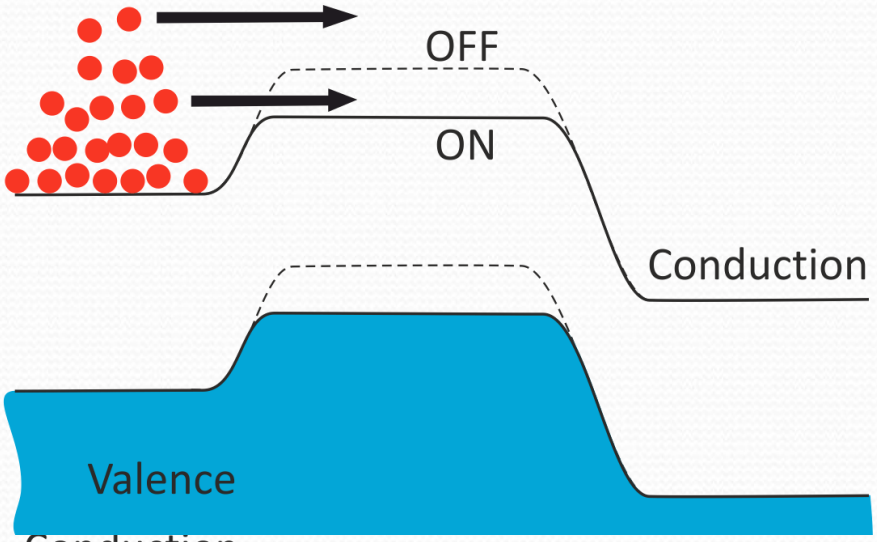
Предельная крутизна переключения: 60 мВ/дек для термоэмиссионого механизма переноса тока

Как сделать круче?

Туннельные транзисторы

позволяют достичь
подпороговой крутизны выше (60мВ/дек)-1
при комнатной температуре

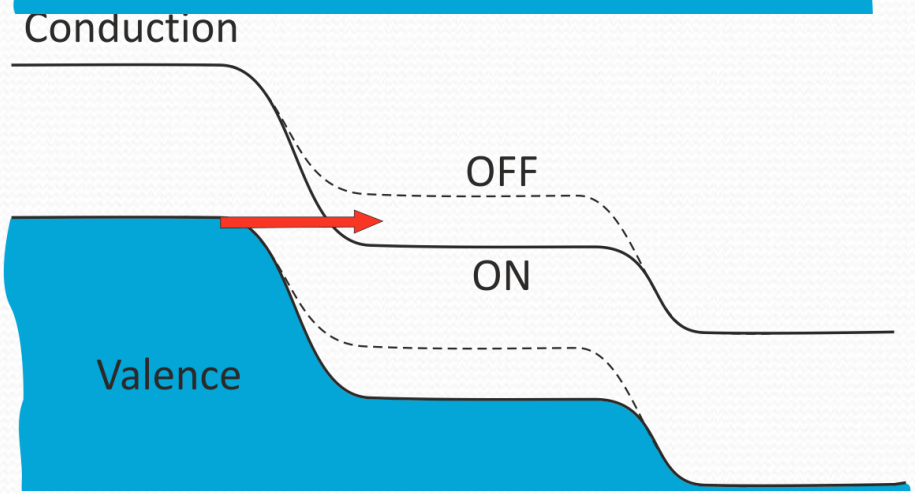
Tunnel FET vs. thermionic FET



$$I \propto \exp\left[-\frac{eV_B}{kT}\right]$$

$$\frac{d\ln I}{dV_G} \le \frac{e}{kT} = \left(60\ \text{mV/dec}\right)^{-1}$$

Limits the drive voltage V_{DD}>240 mV to achieve 4 decade switching



$$I \propto \left[E_v - E_c\left(V_G\right)\right]^{\alpha} \exp\left[-\frac{F_{cr}}{F\left(V_G\right)}\right]$$

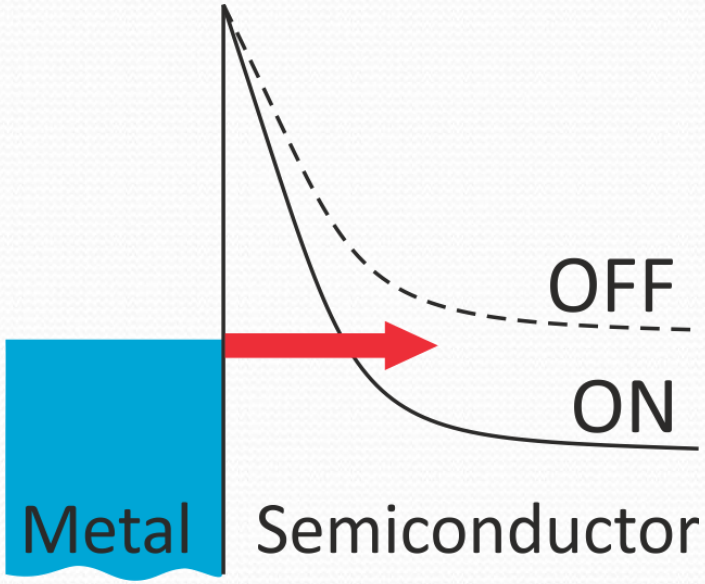
$$\left.\frac{d\ln I}{dV_G}\right|_{E_c \to E_v} \to \infty$$

Low voltage switching possible – low power operation

Tunnel transisors

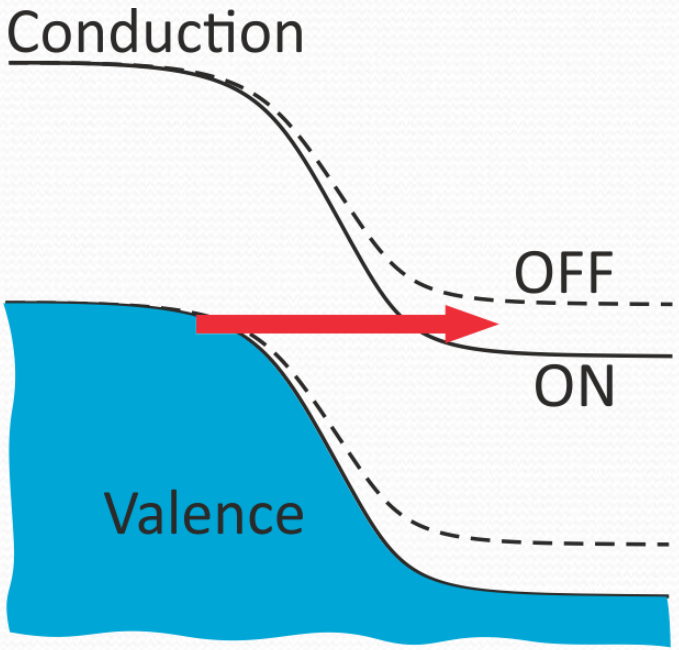
Shottky-barrier FET

- Gate-controlled reverse-biased Shottky junction
- Intraband metal-semiconductor tunneling



Interband tunnel FET

- Gate-controlled reverse-biased Esaki junction
- Valence-to-conduction band tunneling



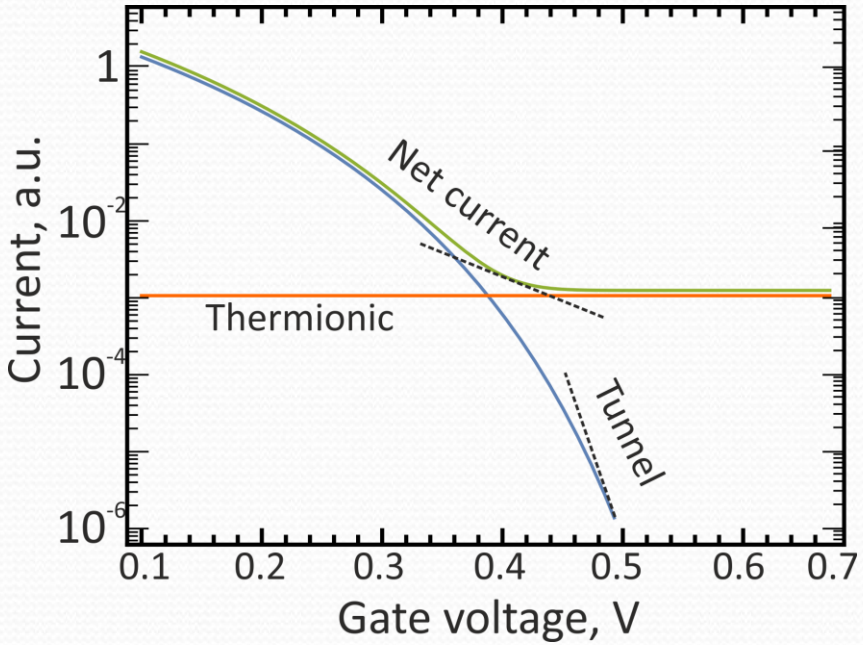
Shottky-barier TFETs: ultimate subthreshold slope

$$I = I_{tun} + I_{therm}$$

$$I_{therm} \propto \exp\left\{-\frac{\Phi_b}{kT}\right\}$$

$$I_{tun} \propto \exp\left\{-\frac{4}{3}\frac{\sqrt{2m\Phi_b^3}}{e\hbar F\left(V_G\right)}\right\}$$

The subthreshold slope of tunnel component is large only when tunnel component is small and masked by thermionic current ➔ The (60 mV/dec)-1 limit persists for SB FET despite the presence of tunneling



Schematic view of current components in SB FET vs gate voltage illustrating the impossibility to achieve subthermal steepness

D. Svintsov et.al. Semiconductors 47, p. 279 (2013)
W. G Vandenberghe. et al. Appl. Phys. Lett. 102, 013510 (2013)

TFETs subthreshold: state of the

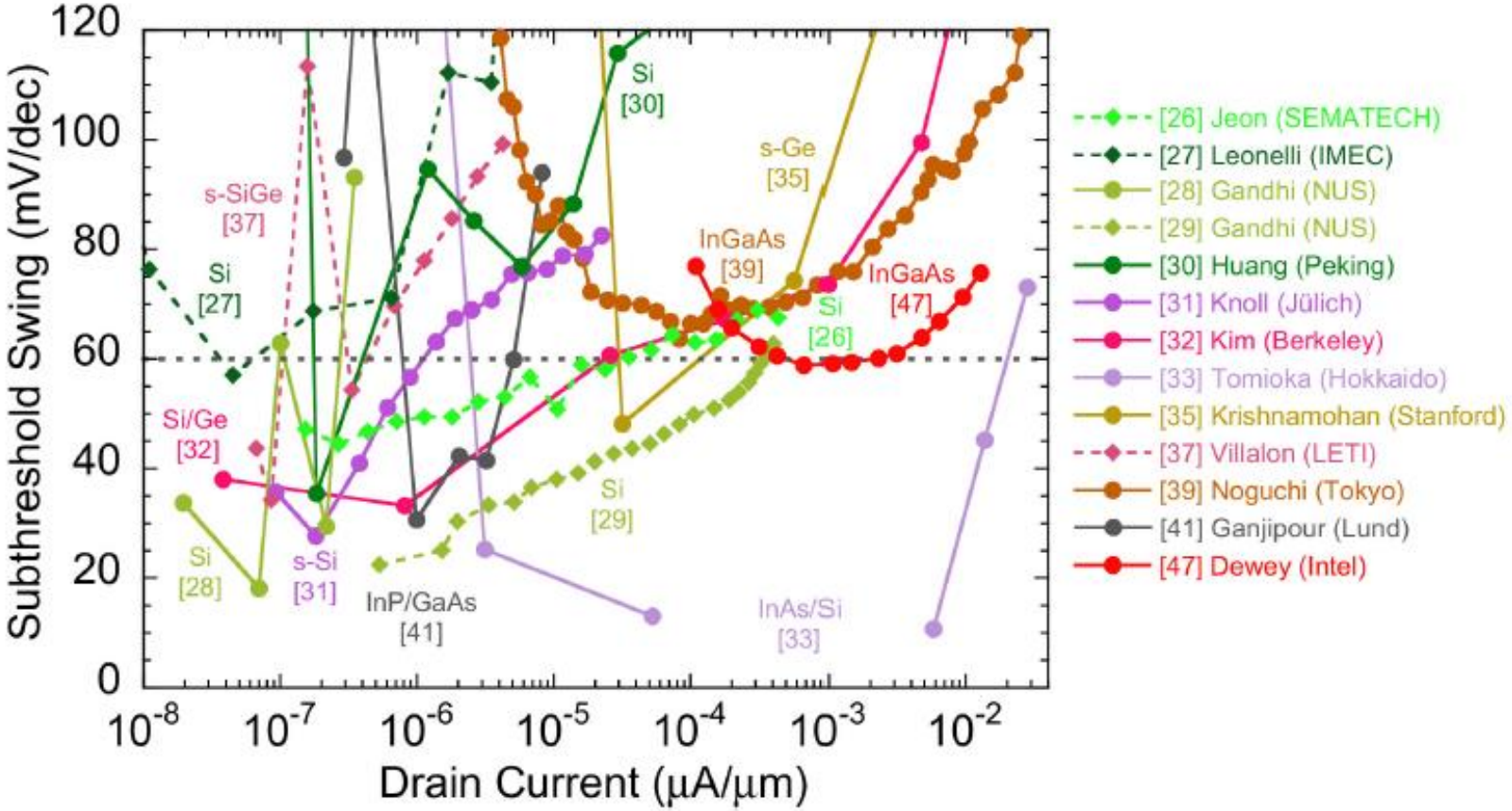
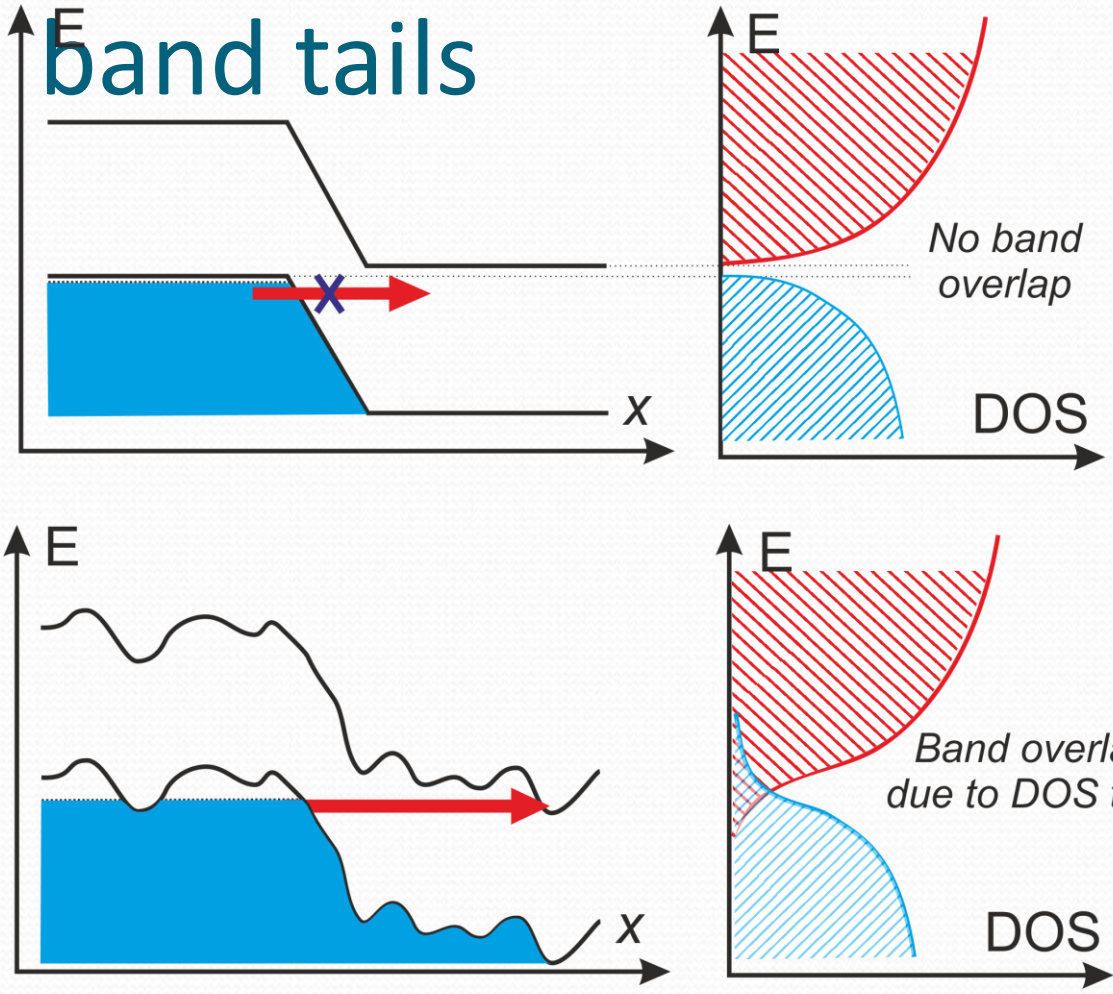


FIGURE 3. Published [26], [29], [31], [32], [37], [39], [47] and extracted [27], [28], [30], [33], [35], [41] TFET sub-threshold swing versus drain current per unit width for *n*-channel (circle with solid line) and *p*-channel (diamond symbol with dashed line) TFETs that show *SS* near or below 60 mV/decade at room temperature. With the exception of the CNT TFETs [48], [49] this is a comprehensive plot showing 12 TFETs with reported SS below 60 mV/decade.

H. Lu ans A.C. Seabaugh IEEE Journal of the Electron Devices Society ***2*** *p. 44-49 (2014)*

Limits of the subthreshold slope:

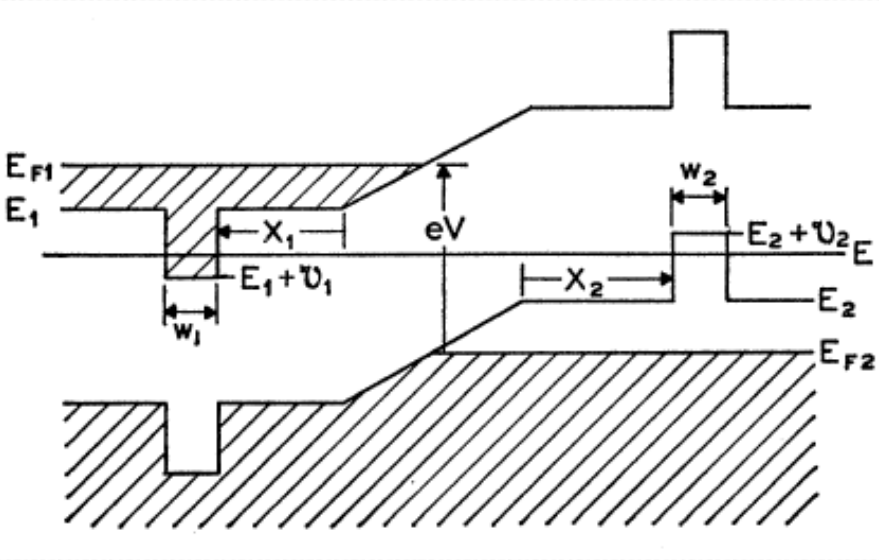
band tails

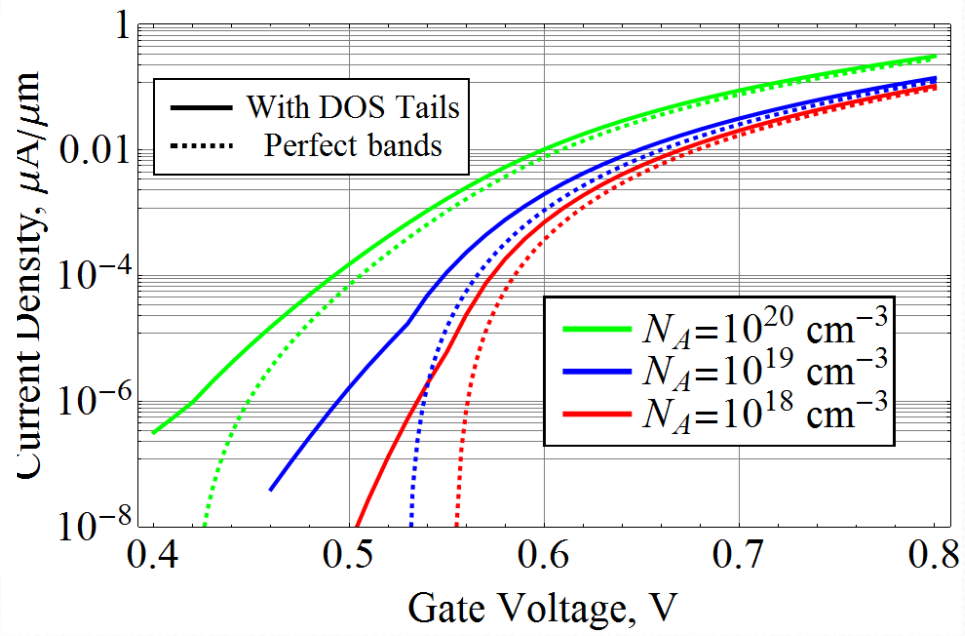


Nonzero current due to tunneling from the DOS tails!

E.O. Kane Phys. Rev. ***131****, (1963)*
S. Mookerjea et. al. IEEE EDL ***31*** *(2010)*
C.D. Bessire et. al. Nano Lett. ***11*** *(2011)*

Limits of the subthreshold slope:
band tails

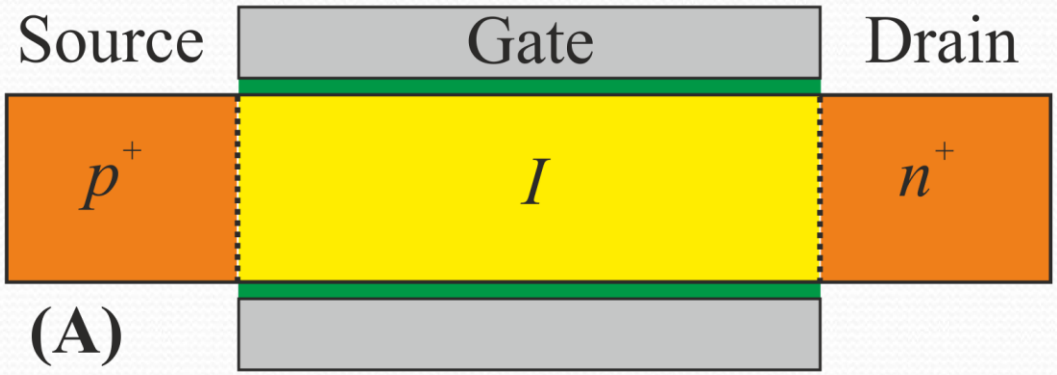


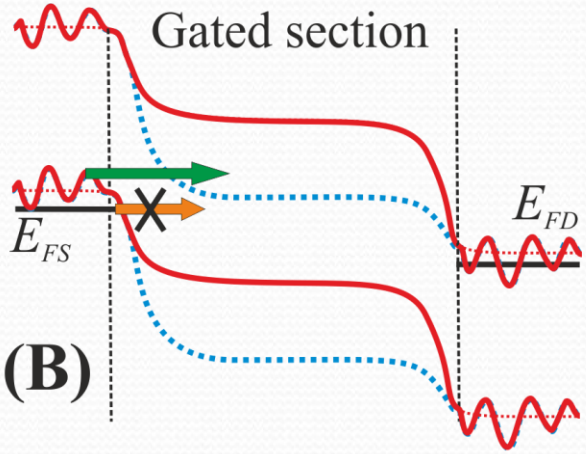


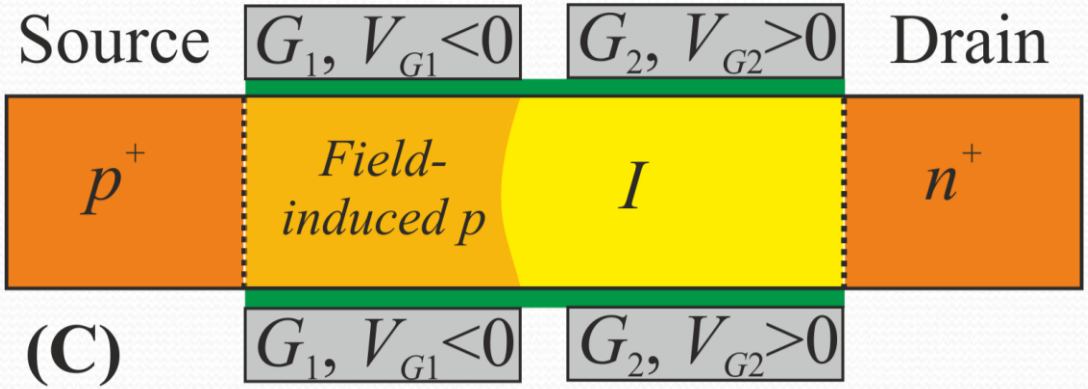
E.O. Kane 1963 *Phys. Rev* ***131*** *p. 79*

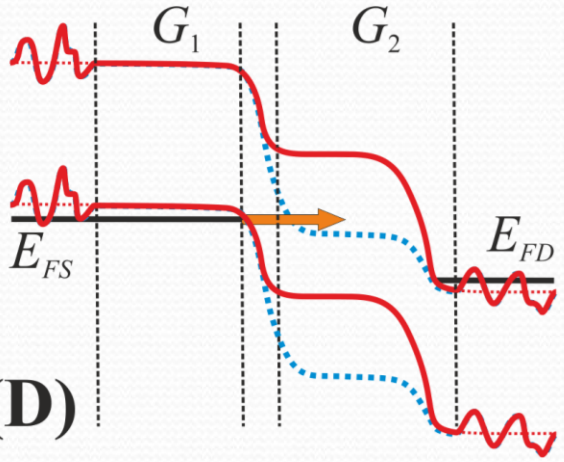
Comparison of TFET modeling with perfectly flat bands (dashed) and taking into account the band tails (solid)

Multigate TFET with electrically induced p-n junction

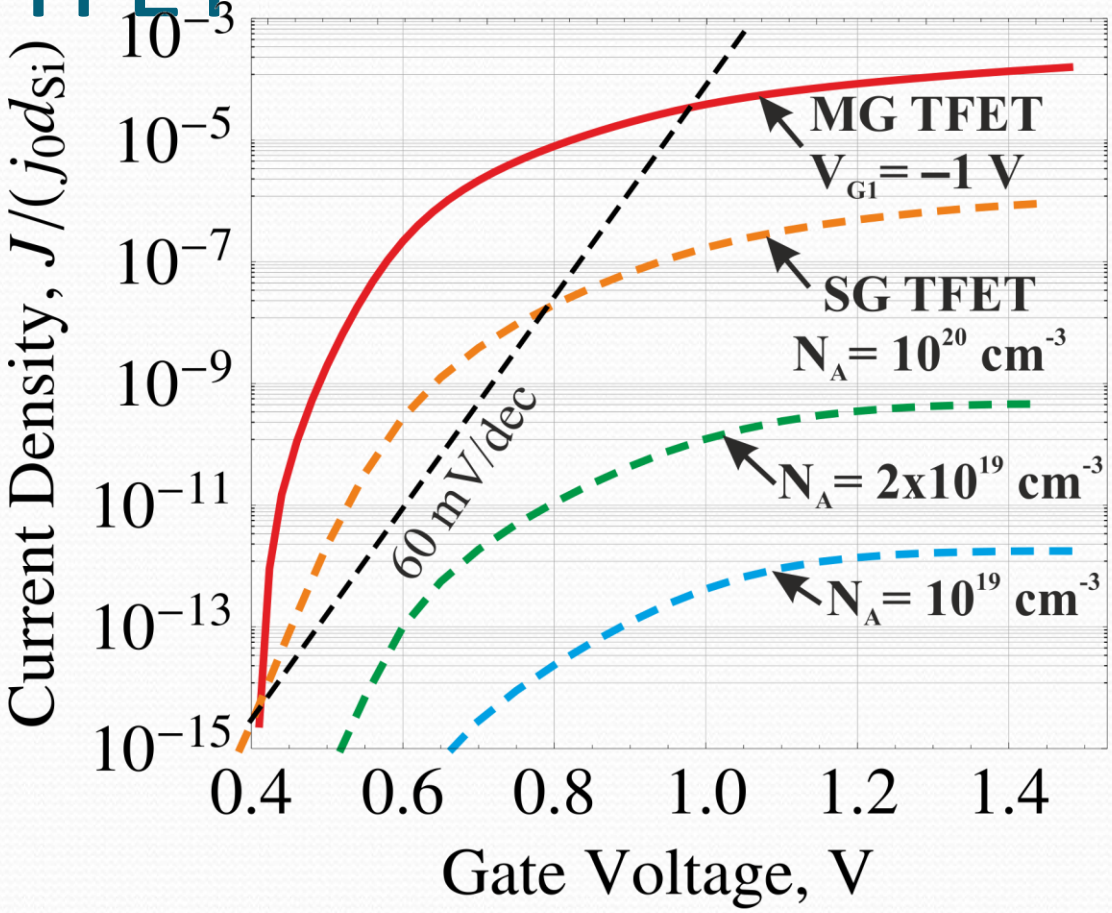








Simulated characteristics of MG-TFET

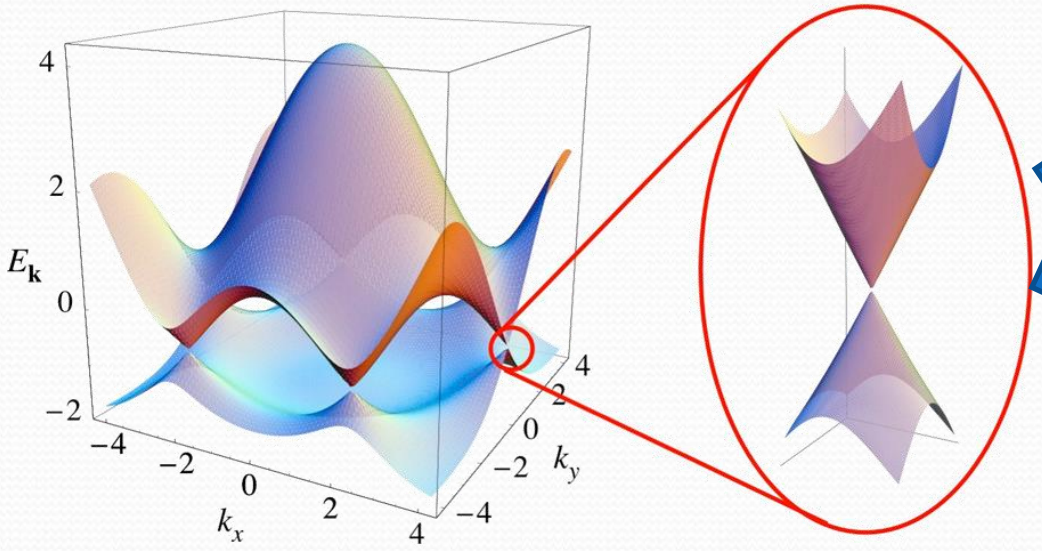


Simulated $I(V_G)$-curve for multigate FET with electrically induced junctions (MG TFET, solid) and common FETs with doped source and drain

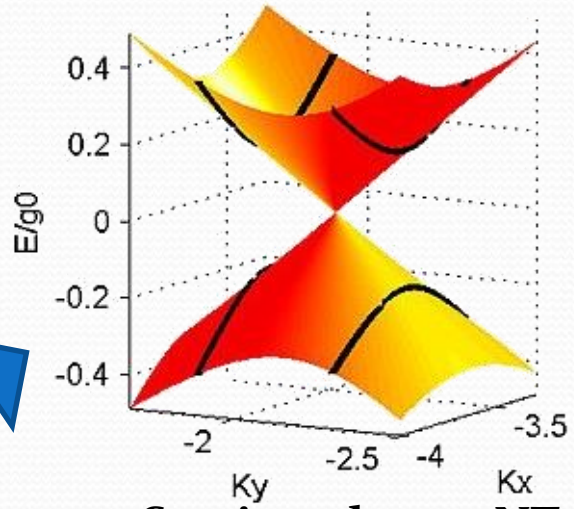
- Gate dielectric 2 nm, κ=25 (e.g. HfO_2);
- Distance between gates ("doping" and "control" gates) is 2 nm;
- 10 nm SOI thickness;
- Better subthreshold due to tunneling in undoped region (no band tails);
- Higher current due to abrupt screening of potential below the "doping" gate.

Graphene FETs

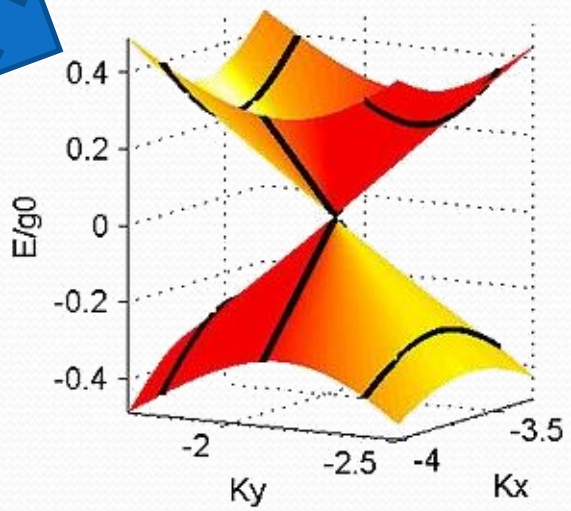
Graphene and nanotubes: electronic properties



Graphene electronic spectrum

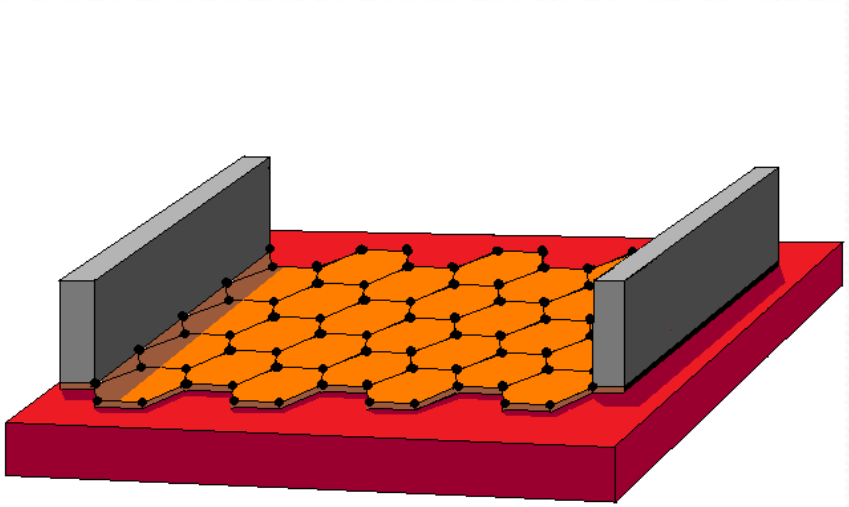


Semiconductor NT

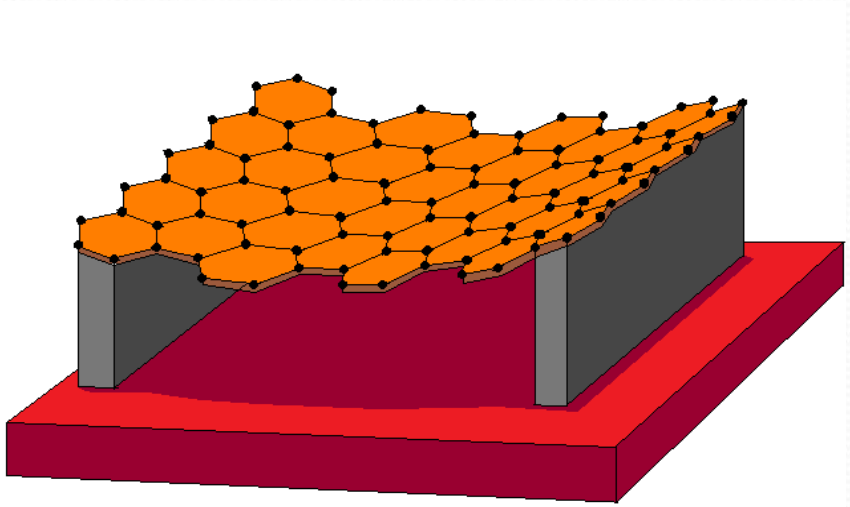


Metallic NT

Graphene structures



Deposited or **epitaxial** (on **SiC or hBN**) graphene: mobility 5000-10000 cm^2/V s due to
interface defects and bulk phonons

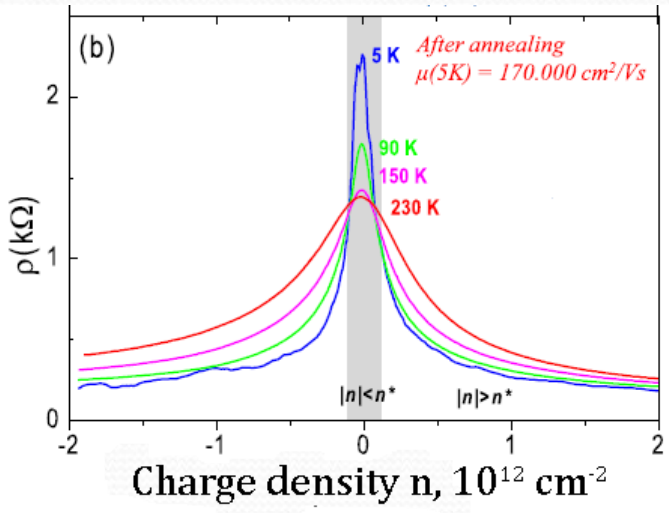


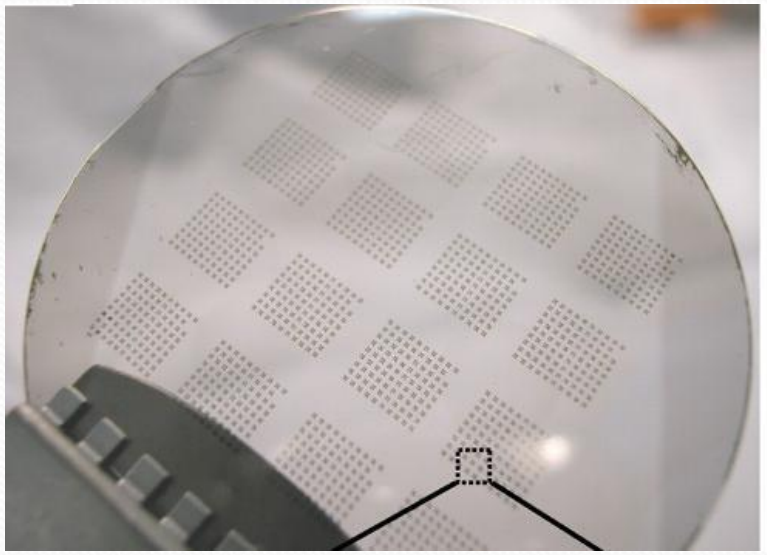
Suspended graphene or twisted graphene stack: mobility 100000-200000 cm^2/V s

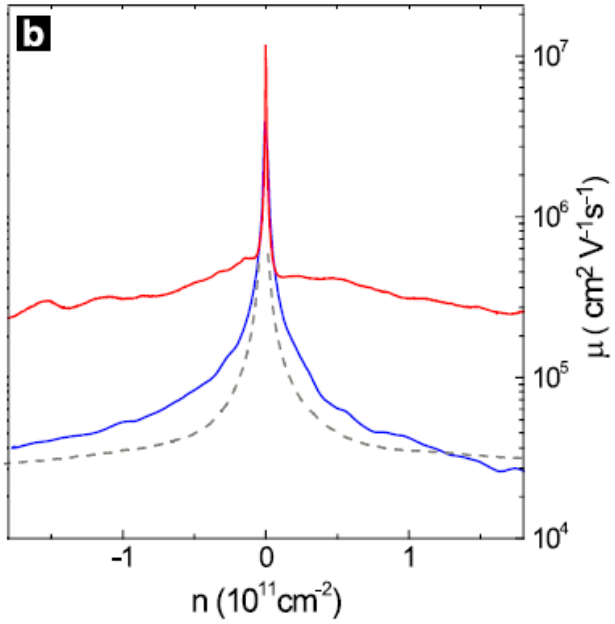
no

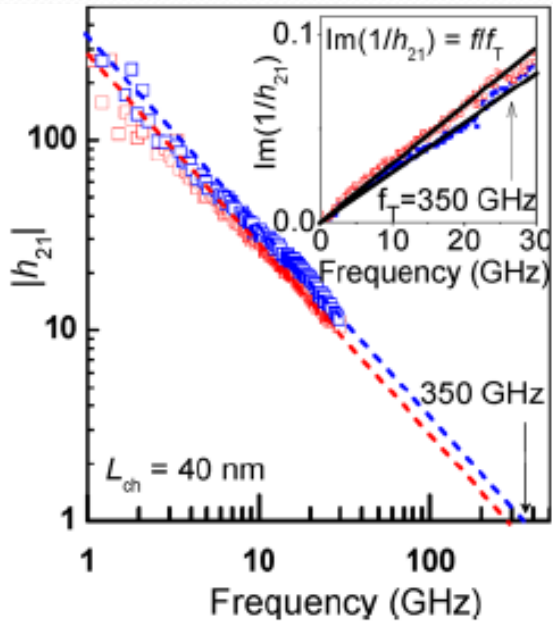
interface defects and bulk phonons

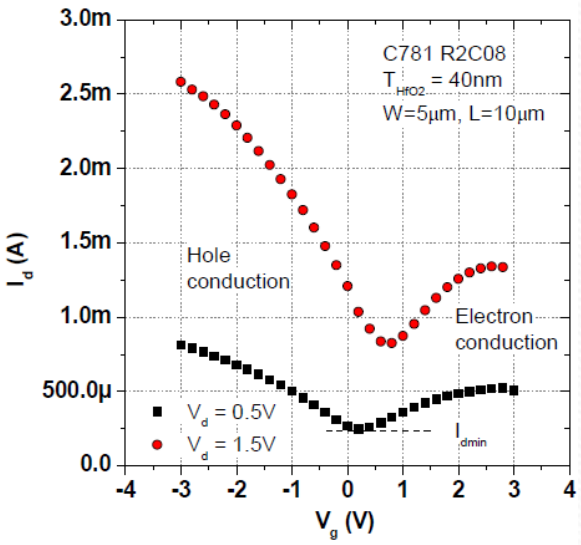
Электронные свойства графена



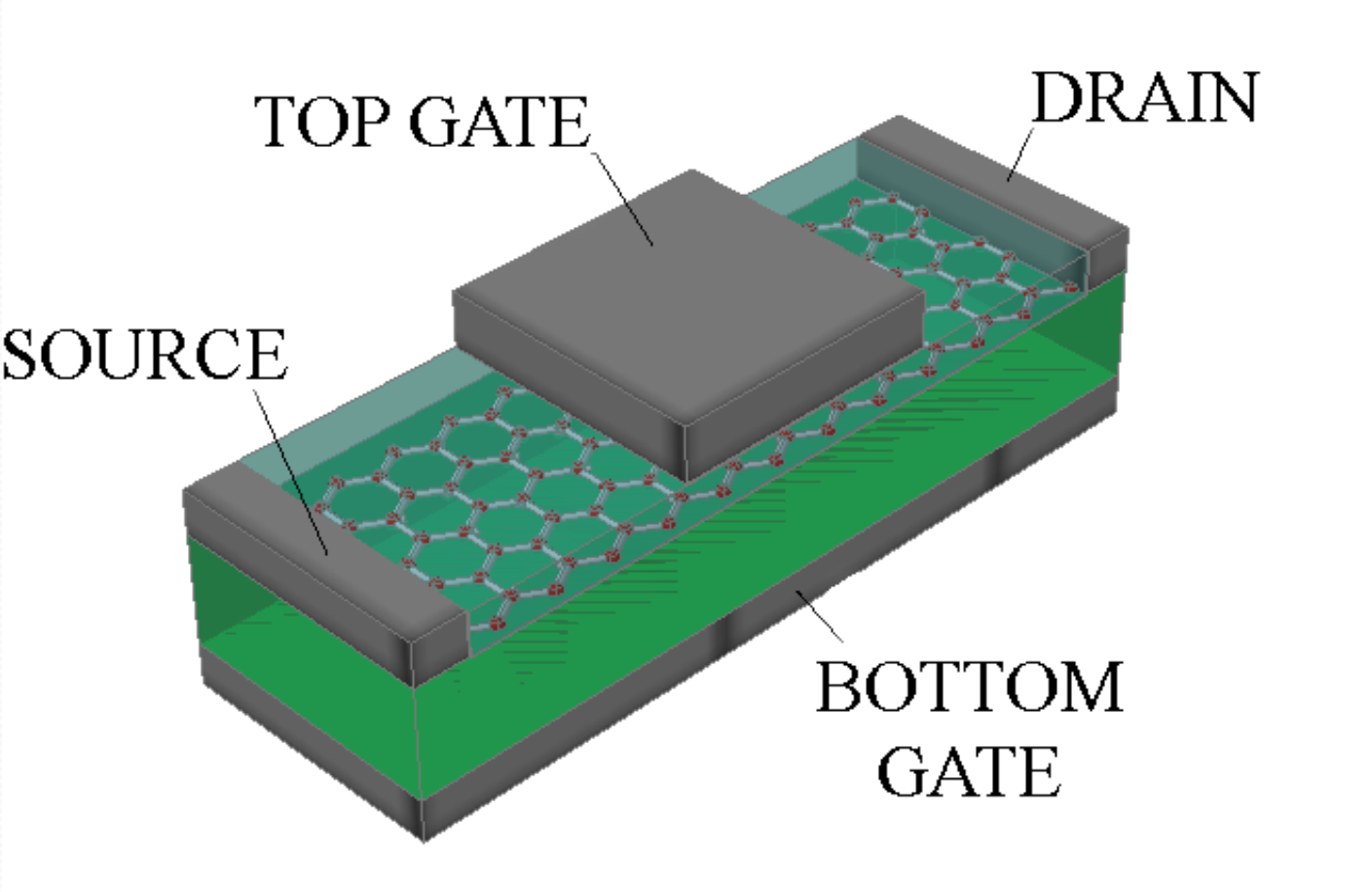








FET structure



Модель транспорта электронов в графене

- Высокая частота межэлектронных столкновений позволяет описывать транспорт в гидродинамической модели

$$\frac{\partial(\rho_e u_e)}{\partial t}+\frac{\partial}{\partial x}\left(\frac{\varepsilon_e}{2}\left[1+2\left(\frac{u_e}{v_F}\right)^2\right]\right)-en_e\frac{\partial\varphi}{\partial x_i}=-\beta_{e-i}u_e-\beta_{eh}(u_e-u_h),$$

$$\frac{\partial(\rho_h u_h)}{\partial t}+\frac{\partial}{\partial x}\left(\frac{\varepsilon_h}{2}\left[1+2\left(\frac{u_h}{v_F}\right)^2\right]\right)+en_h\frac{\partial\varphi}{\partial x_i}=-\beta_{h-i}u_h-\beta_{eh}(u_h-u_e).$$

n_e, n_h – electron and hole concentrations

ρ_e, ρ_h – electron and hole mass densities $\rho \neq nm_0$

u_e, u_h – drift velocities

β_{e-i}, β_{h-i} – friction coefficients

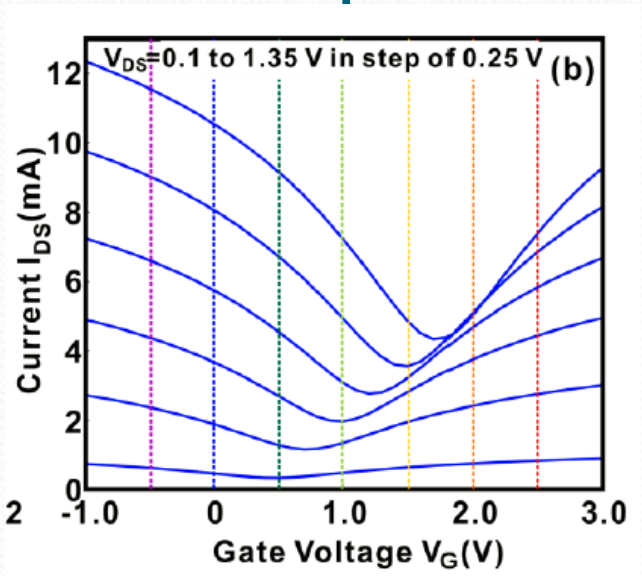
$$n=\frac{n_0}{\left[1-(u/v_F)^2\right]^{3/2}},\ \rho=\frac{\rho_0}{\left[1-(u/v_F)^2\right]^{5/2}}$$

D. Svintsov, V. Vyurkov, S. Yurchenko, V. Ryzhii, T. Otsuji *"Hydrodynamic model for electron-hole plasma in graphene"*, Journal of Applied Physics, Vol. 111, p. 083715 (2012)

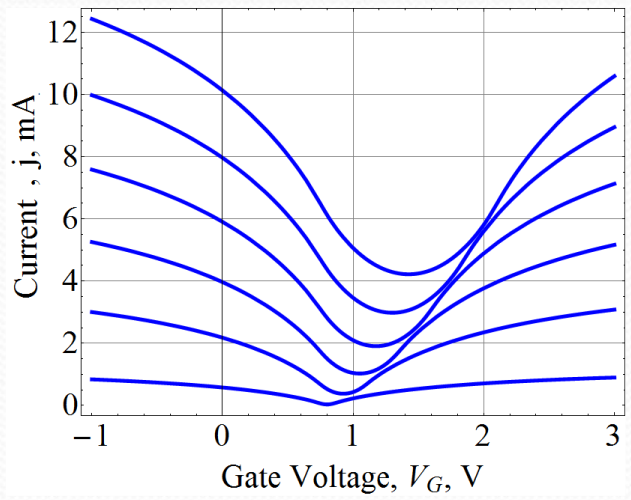
D. Svintsov, V. Vyurkov, V. Ryzhii, T. Otsuji "*Hydrodynamic electron transport and nonlinear waves in graphene*", Physical Review B, Vol. **88**, p. 245444 (2013)

Моделирование характеристик полевых транзисторов

Эксперимент



Теория



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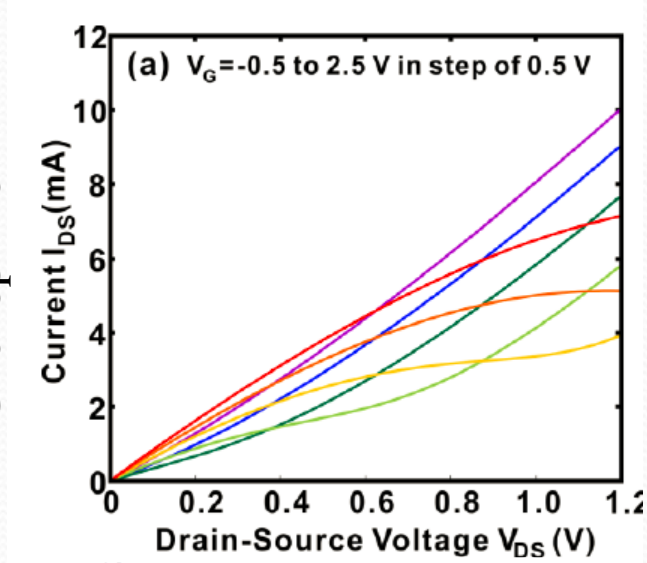

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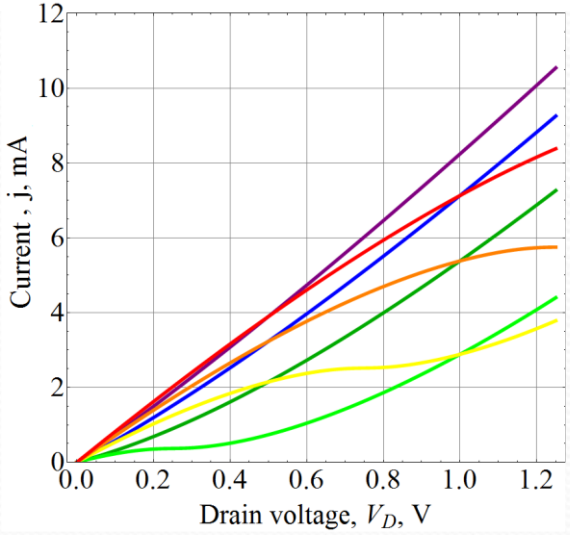
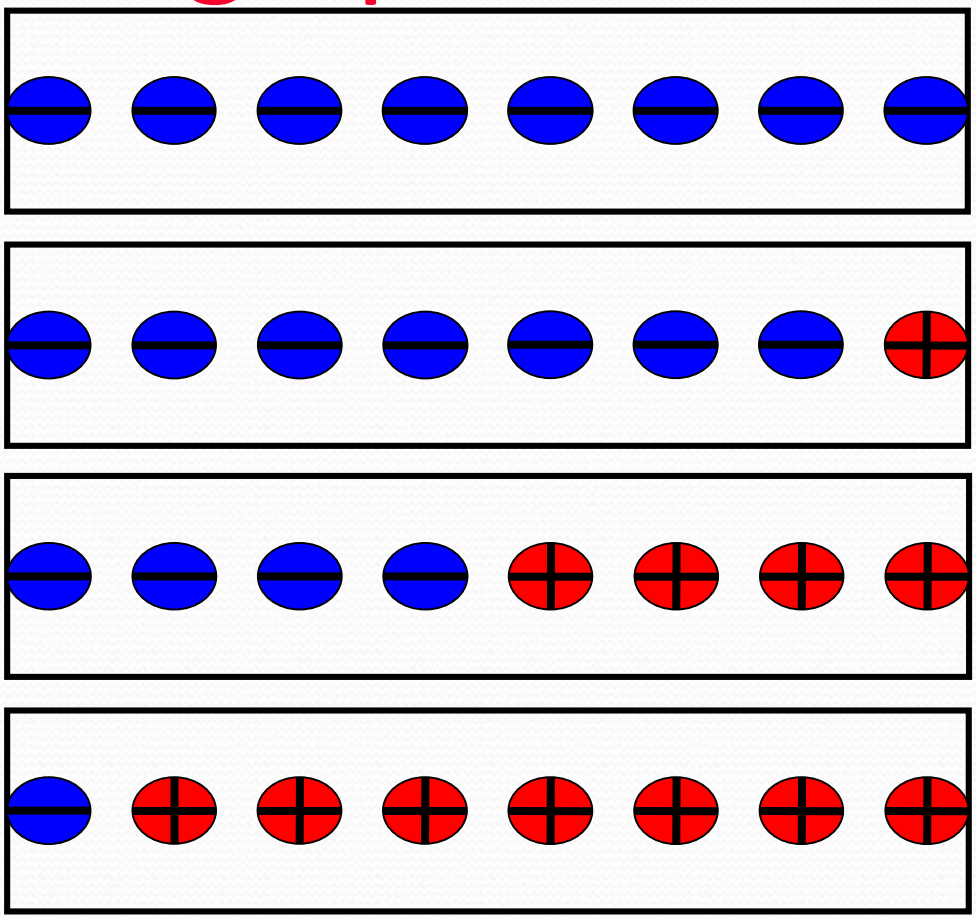


Bipolar graphene FET channel



$V_d < V_g$

$V_d > V_g$

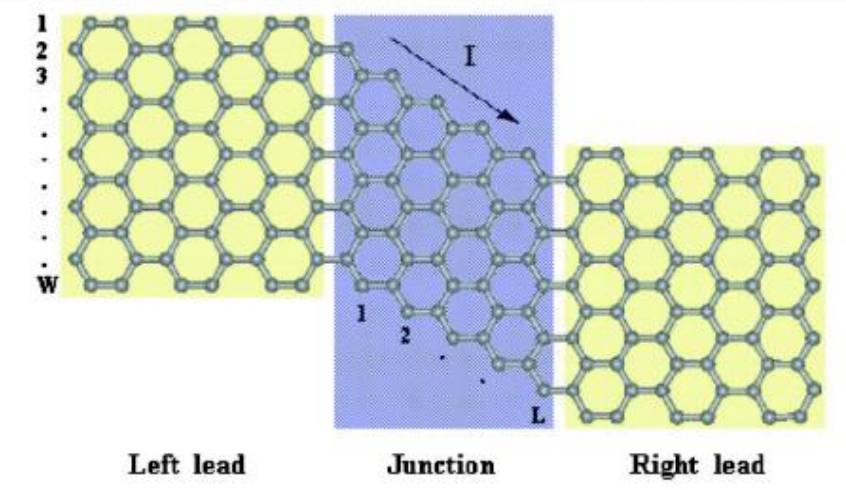
$V_d = 2V_g$

$V_d > 2V_g$

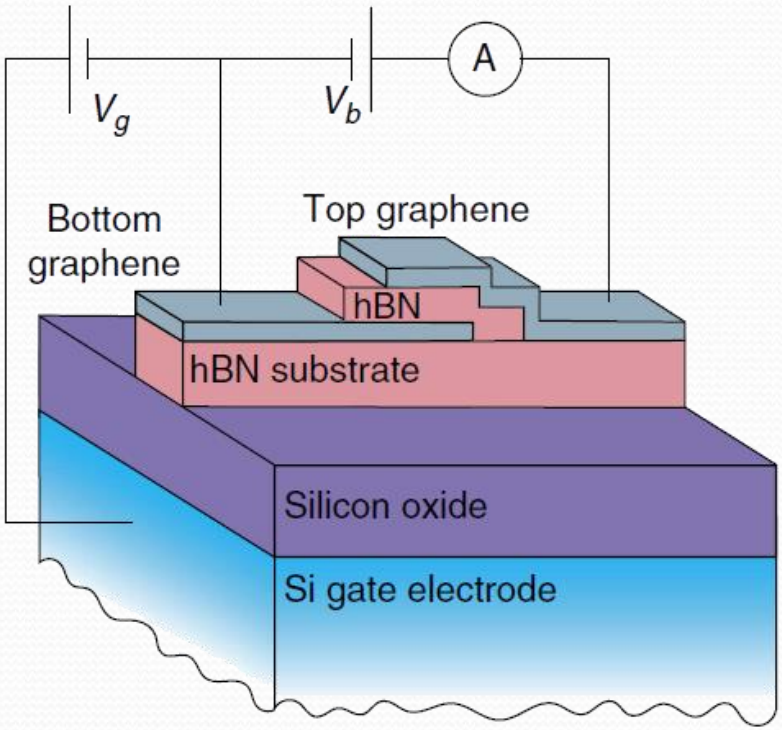
Possible applications: Logic circuits?

- **Graphene**
- => **good** Ohmic source
- and drain contact
- **Gap=o**
- => **big** OFF-state current

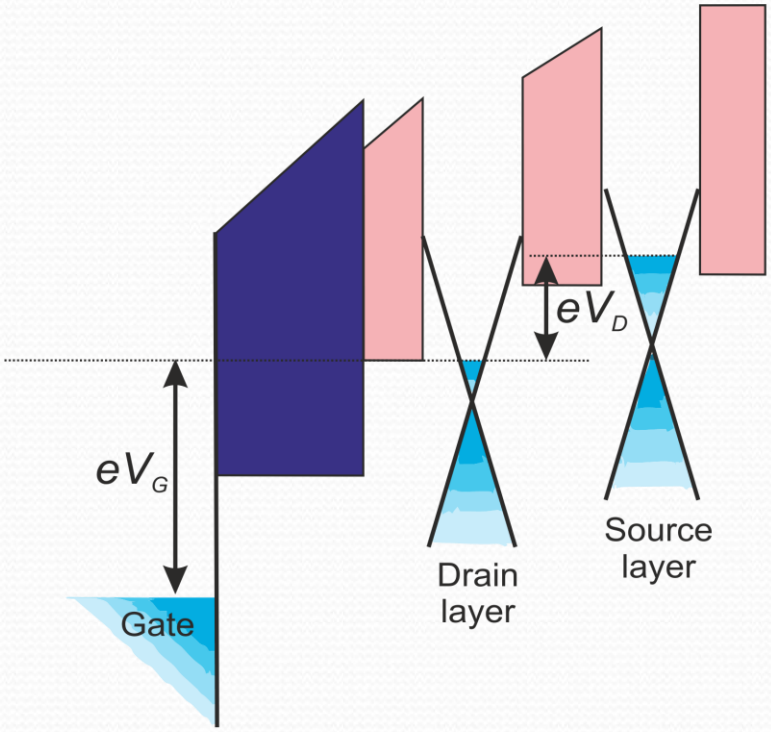
- **Bilayers, nanoribons or graphane**
- => **bad** Ohmic source and
- drain contact
- **Gap≠o**
- => **low** OFF-state current



Graphene vertical tunnel FETs



Layout of vertical graphene tunnel FET. Tunneling occurs between two graphene layers separated by 3-10 monolayers of boron nitride

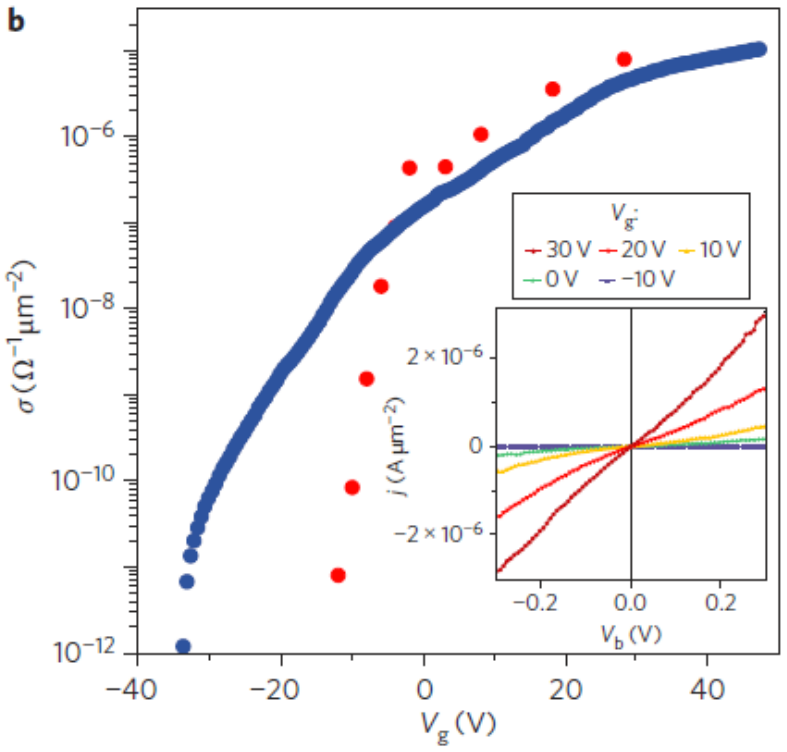


Band diagram of graphene lateral TFET. The gate voltage controls the tunnel density of states, but not the barrier height

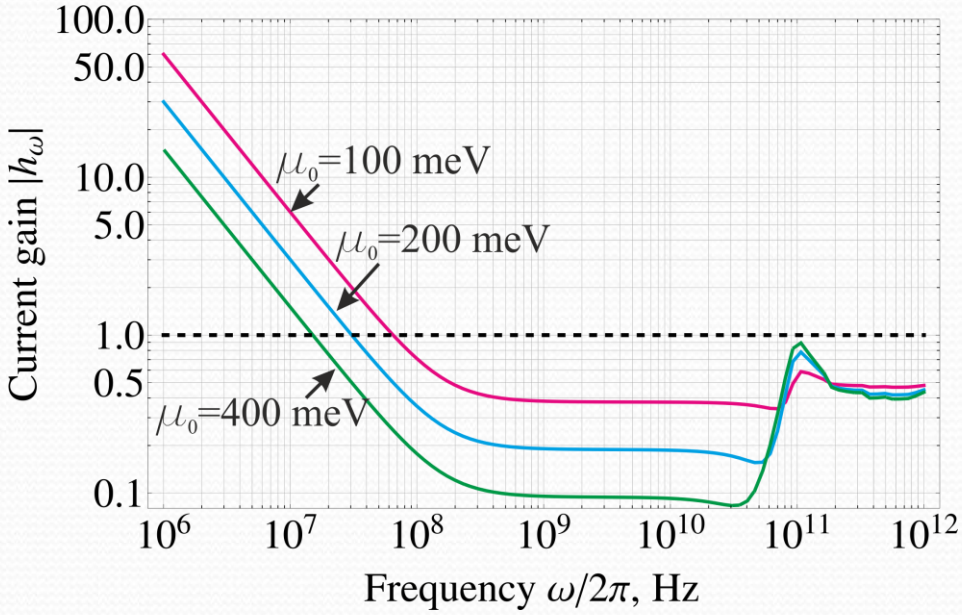
L. Britnell et al ,Science vol. ***335 p. 947 (****2012****)***

L. Britnell et. al., Nature Communications vol. ***4*** *art. no. 1794 (2013)*

Graphene vertical tunnel FETs



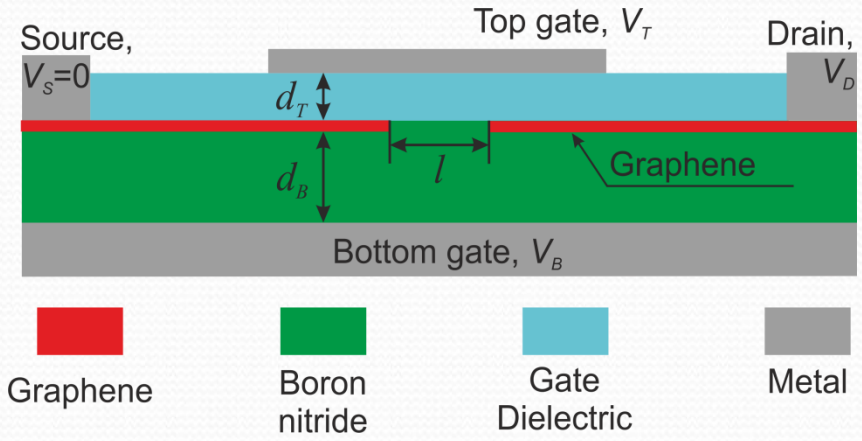
Measured tunnel conductivity of vertical graphene TFET vs. gate voltage



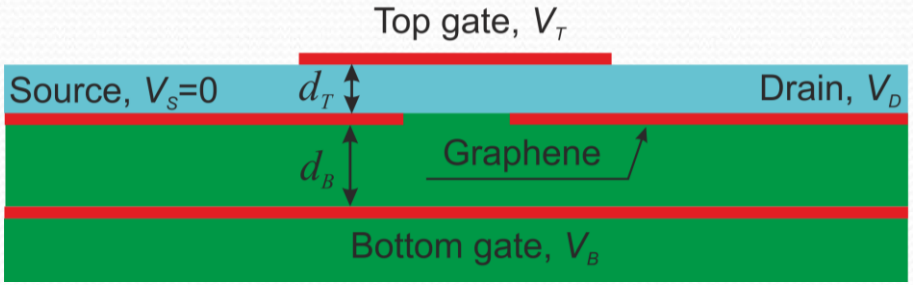
Calculated current gain of vertical graphene TFET vs. frequency at different electron Fermi energies in source layer. Cutoff frequency ~10MHz expected due to small tunneling probability

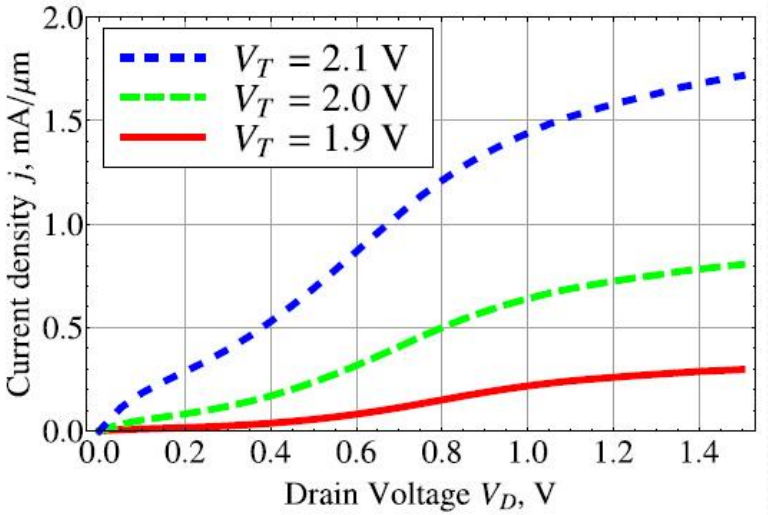
*L. Britnell et. al., Science **335** p. 947 (2012)*
*T. Georgiou et. al. Nature Nanotechnology **8** p. 100 (2013)*
*A. Mishchenko et. al. Nature Nanotechnology **9** p. 808 (2014)*

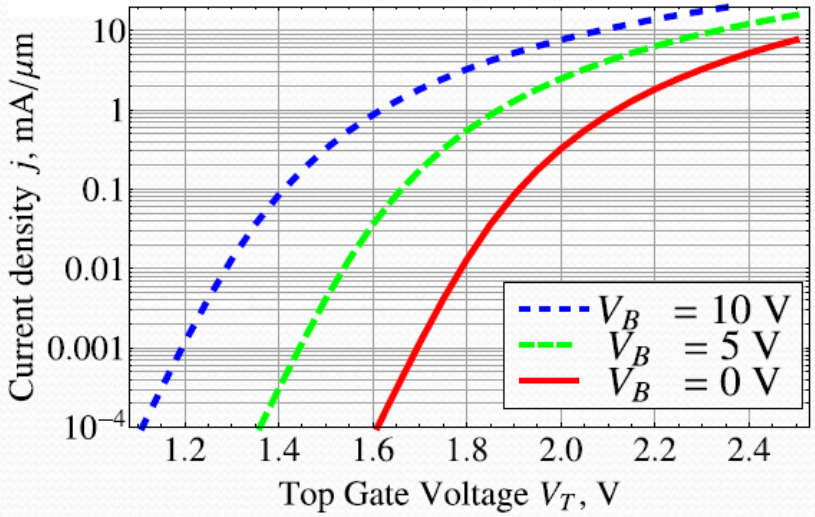
Латеральный туннельный транзистор на основе графена



Структуры предлагаемых транзисторов



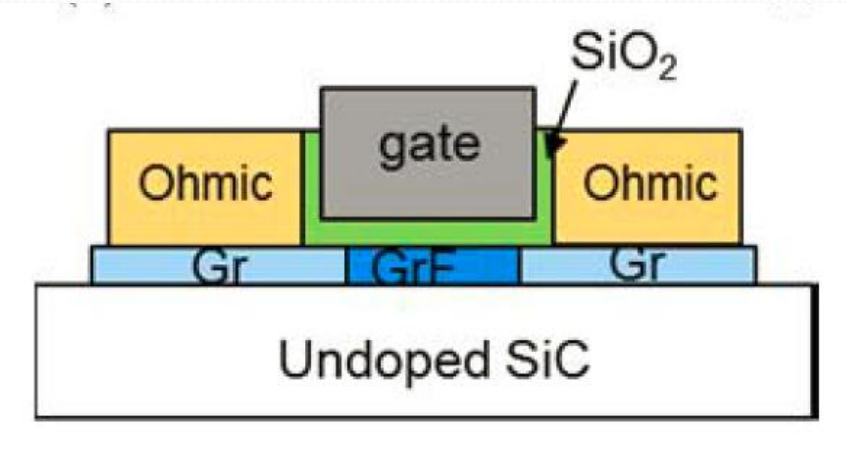


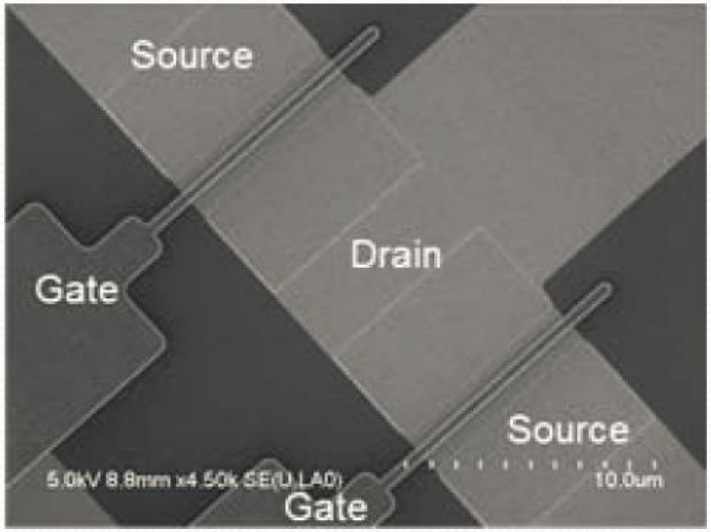


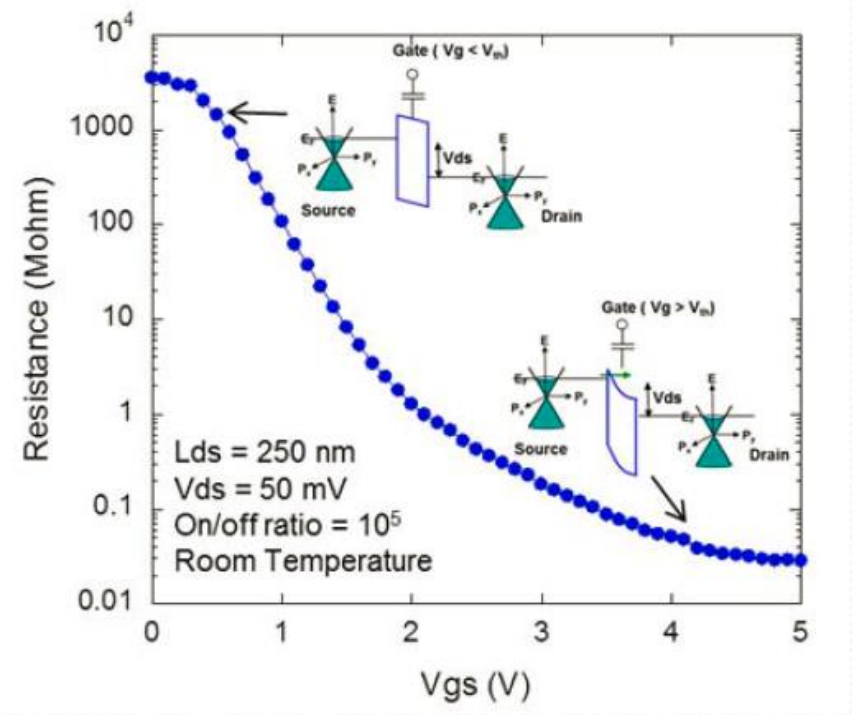
Рассчитанные характеристики, демонстрирующие насыщение тока и высокое (>10^4) отношение токов открытого и закрытого состояний

D. Svintsov *et. al.*, Semiconductors vol. **47**, p. 279-284 (2013)
D. Svintsov *et. al.*, J. Phys. D: Appl. Phys. Special issue “Graphene devices” (2014)

Lateral graphene FET: realization

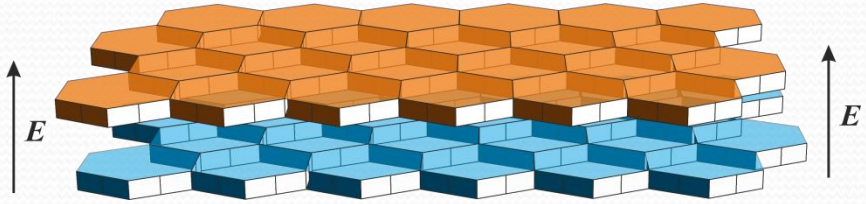


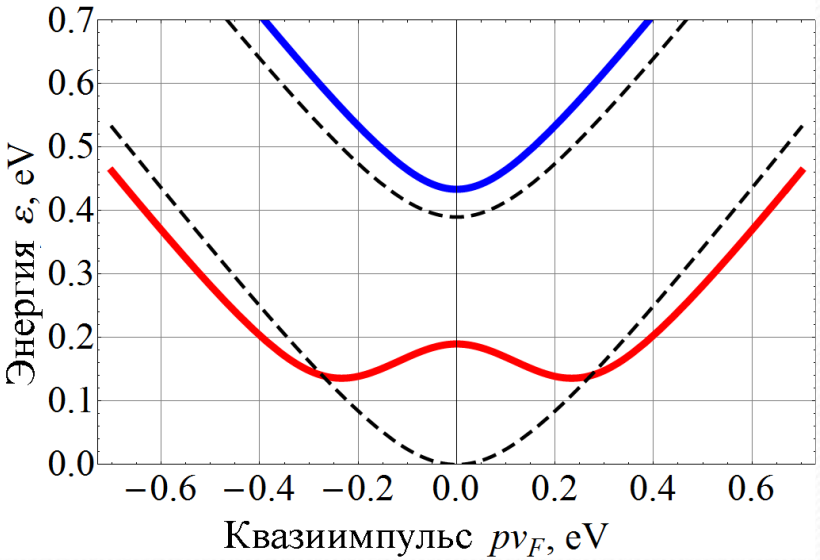




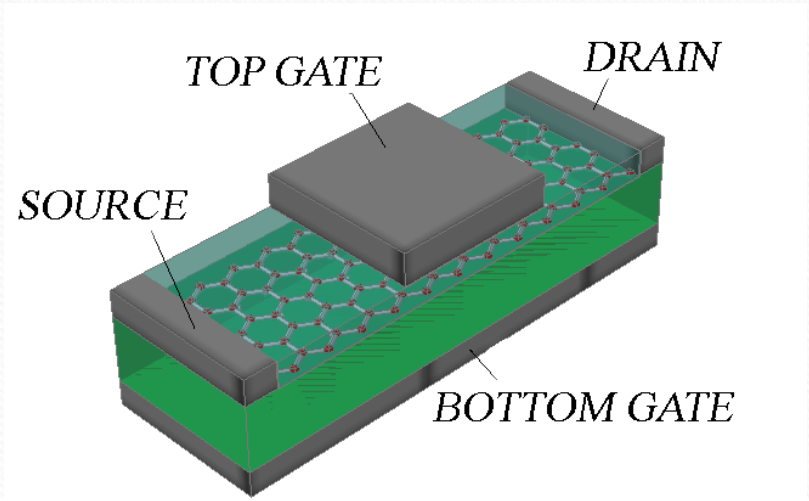
*J.S. Moon et. al. IEEE EDL **34** (2013)*

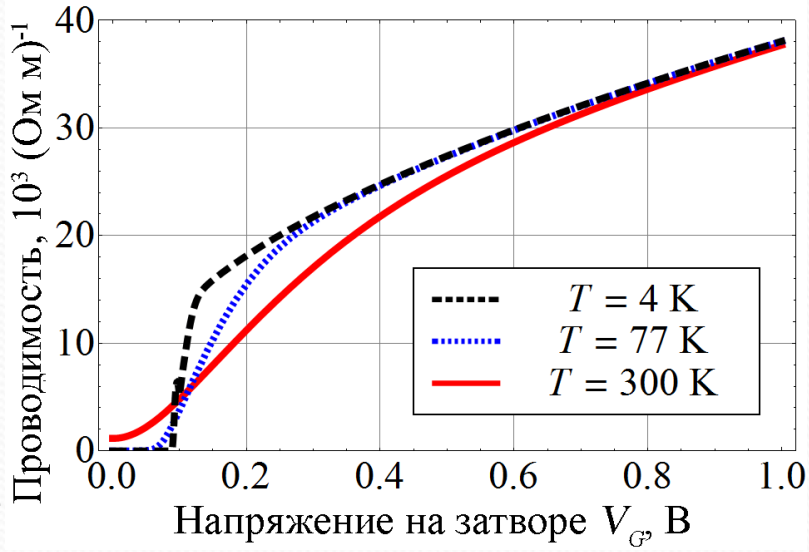
Транзисторы на основе двухслойного графена





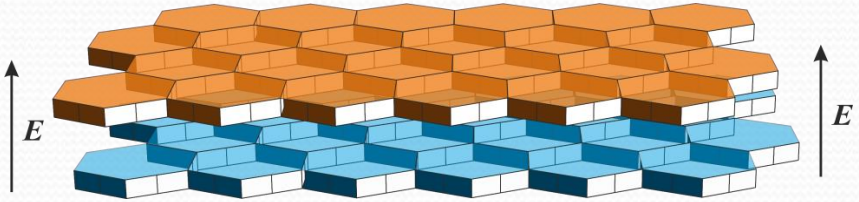
$$\varepsilon^2(p) = \frac{\gamma_1^2}{2} + \frac{\Delta^2}{4} + p^2 v_F^2 \pm \sqrt{\frac{\gamma_1^4}{4} + p^2 v_F^2 \left(\gamma_1^2 + \Delta^2\right)}$$

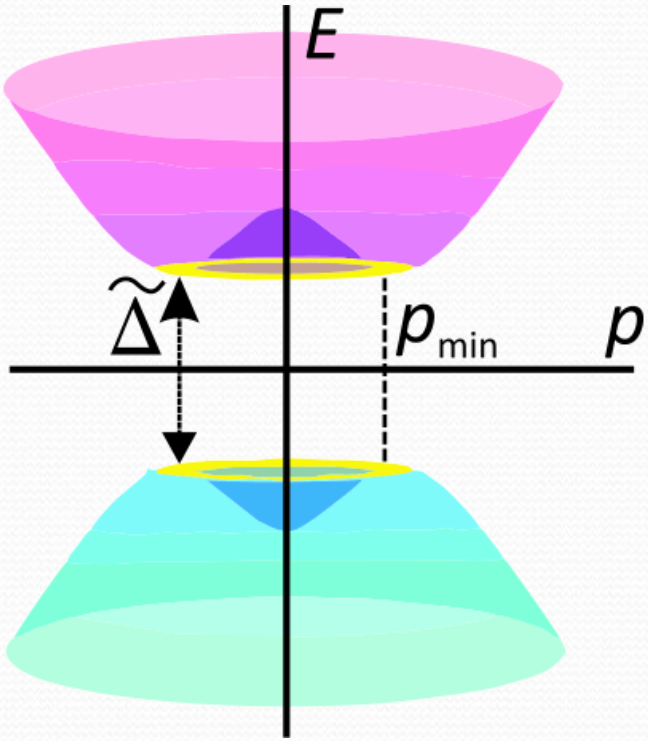




D. Svintsov, V. Vyurkov, V. Ryzhii, T. Otsuji *"Effect of "Mexican Hat" on Graphene Bilayer Field-Effect Transistor Characteristics"*, Japanese Journal of Applied Physics, Vol. 50, Iss. 7, p. 070112 (2011)

Graphene bilayer

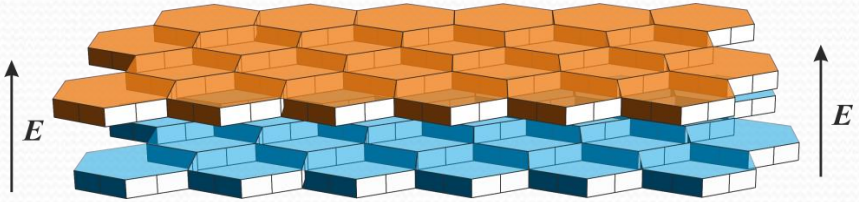




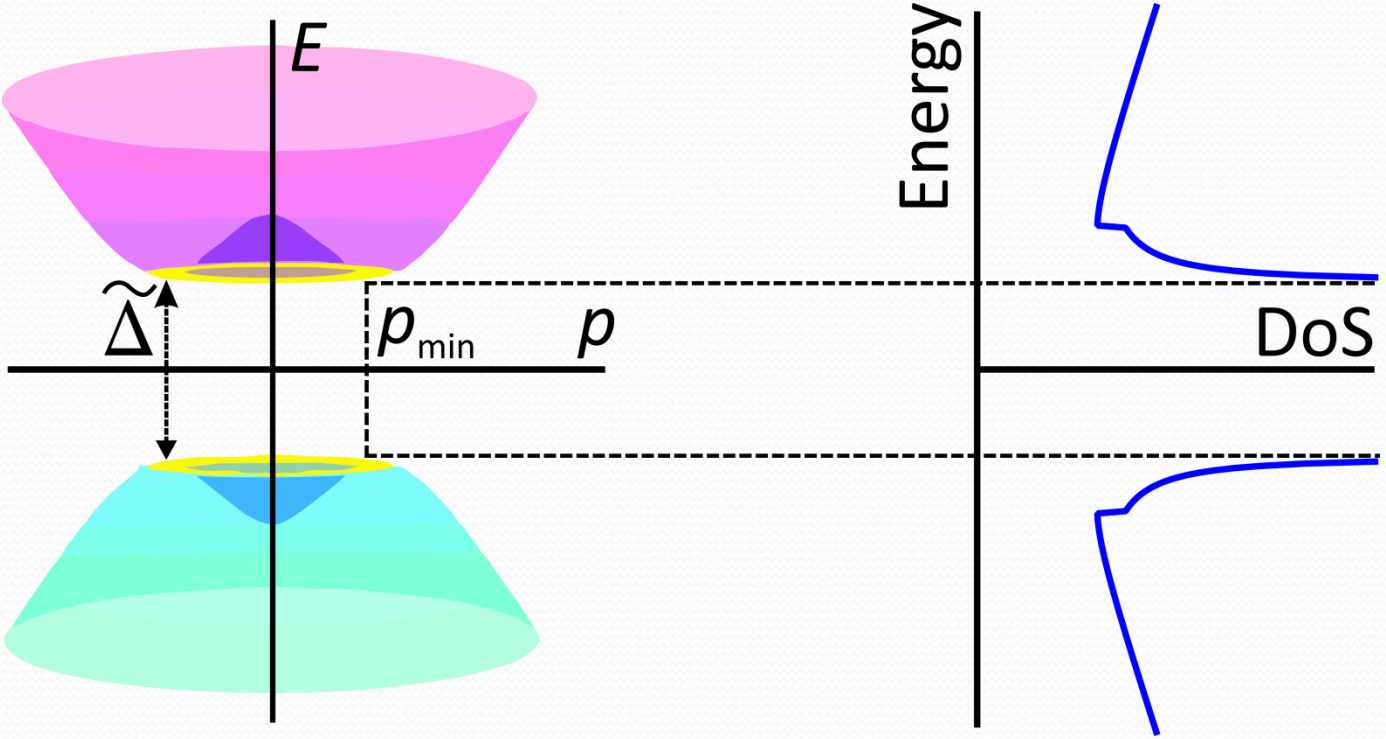
Conduction and valence band electron dispersions in graphene under applied transverse electric field

- Gap opening up to ~0.4 eV by transverse electric field;
- Symmetric "Mexican-hat" band dispersion

Graphene bilayer



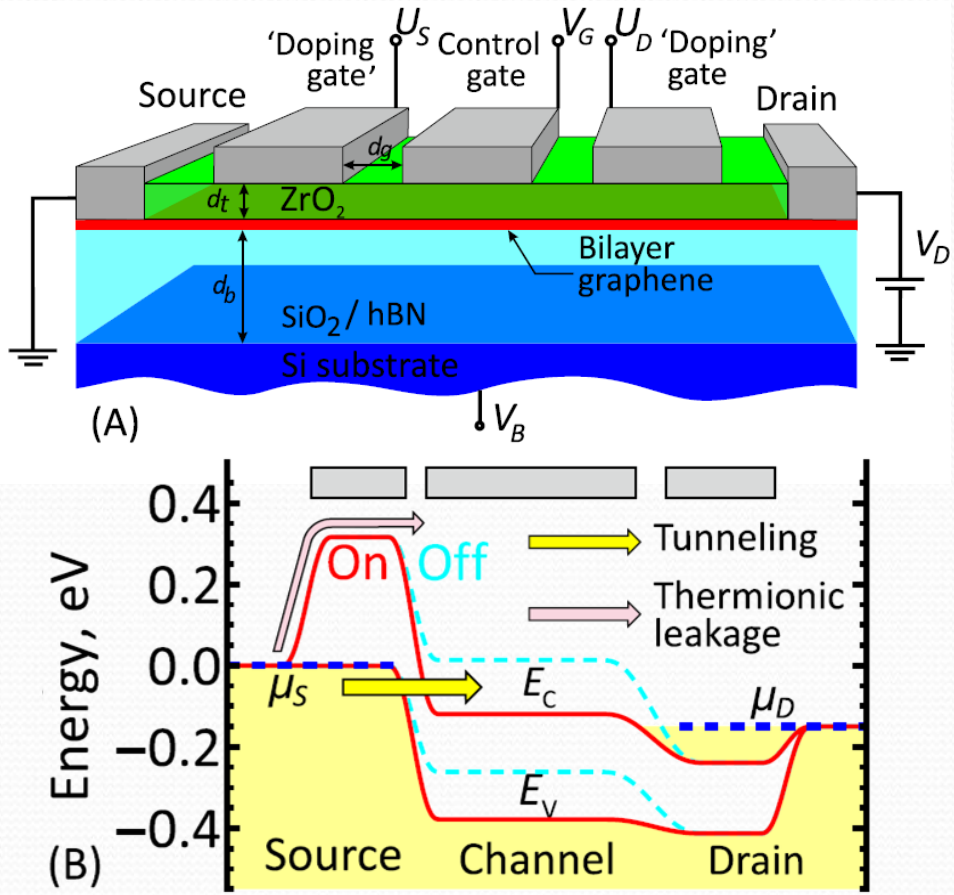
- Gap opening up to ~0.4 eV by transverse electric field;
- Symmetric "Mexican-hat" band dispersion



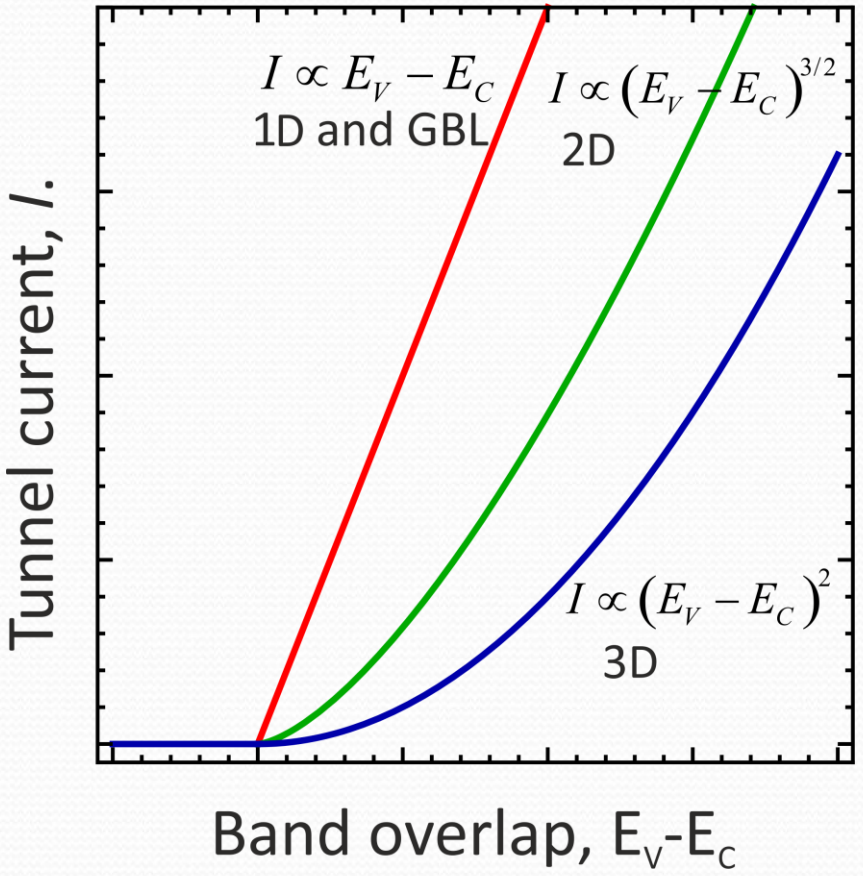
Conduction and valence band electron dispersions in graphene under applied transverse electric field

Density of states in gapped graphene bilayer demonstrating a van Hove singularity

Exploiting the van Hove singularity in tunneling

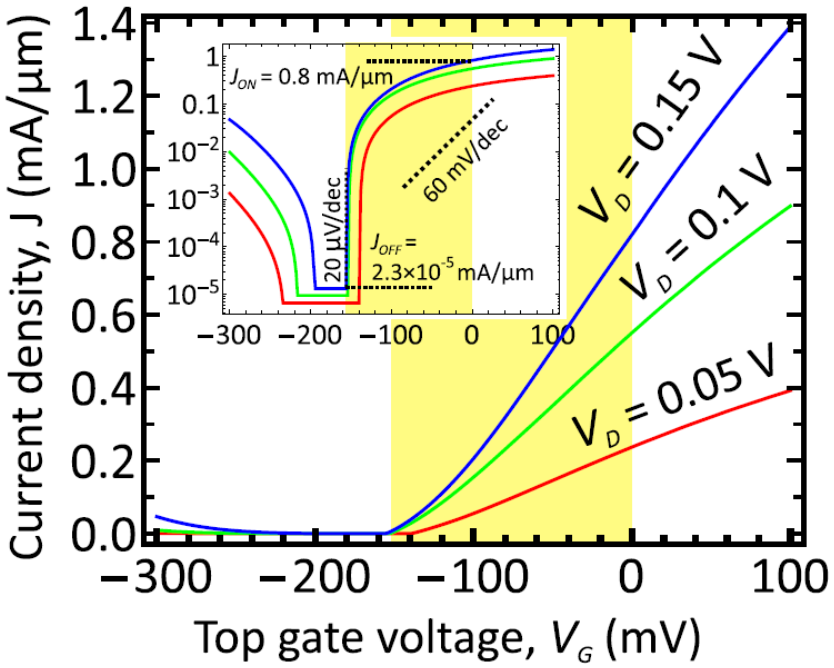


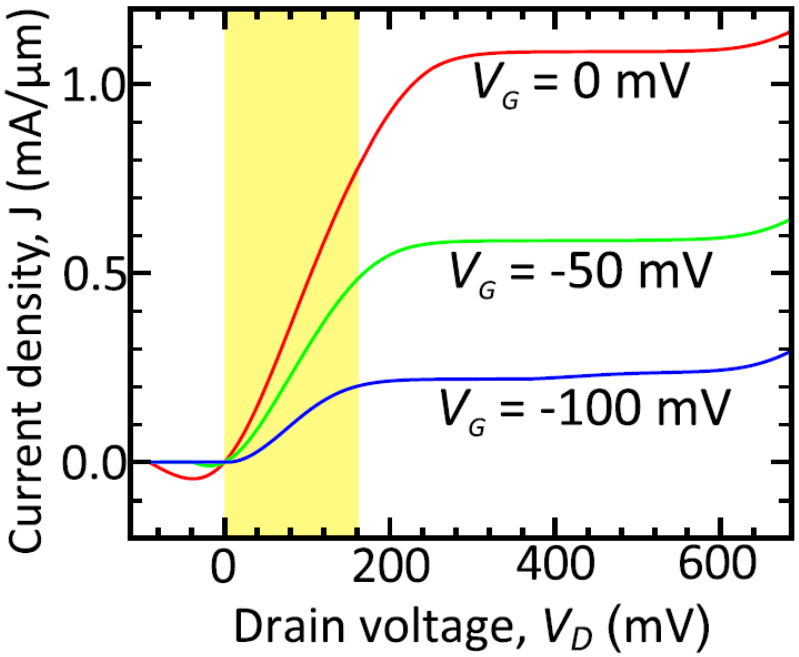
(A) Layout of the proposed graphene bilayer TFET with electrically defined source and drain regions (B) Band diagram of graphene bilayer TFET for the optimal biasing conditions: $V_B > 0$, $U_S < 0$, $U_D > 0$. At zero top gate bias, $V_G = 0$, the TFET is switched on, while at $V_G < 0$ it is switched off.



Schematic dependence of direct interband tunneling current on the band overlap in parabolic band semiconductors of different dimensionality (3D, 2D, 1D) and graphene bilayer.

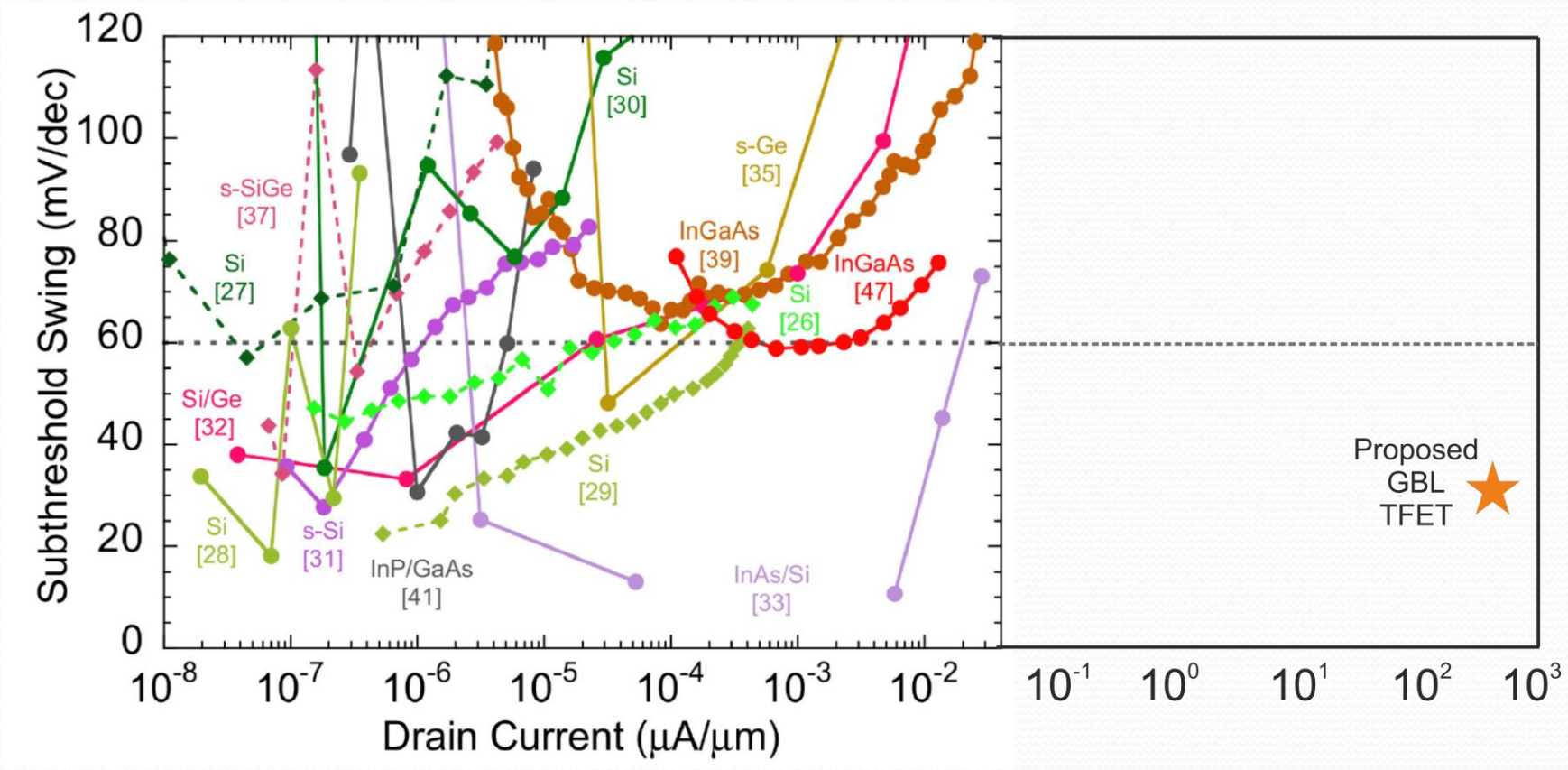
Graphene bilayer TFET characteristics



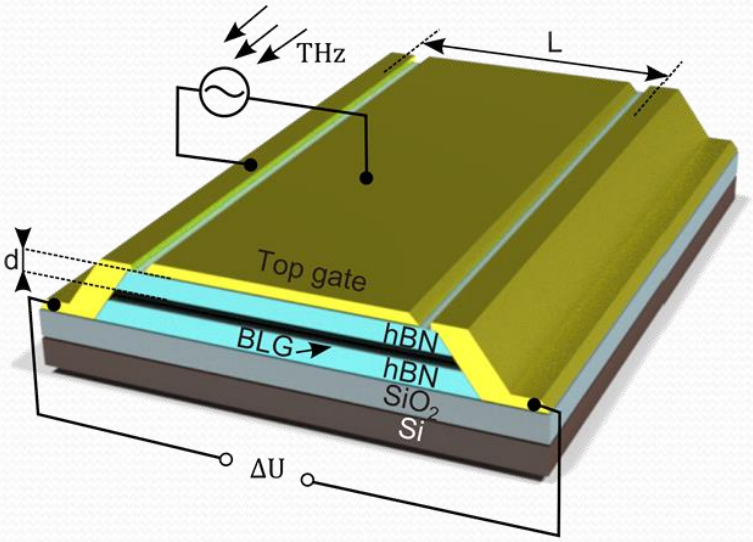


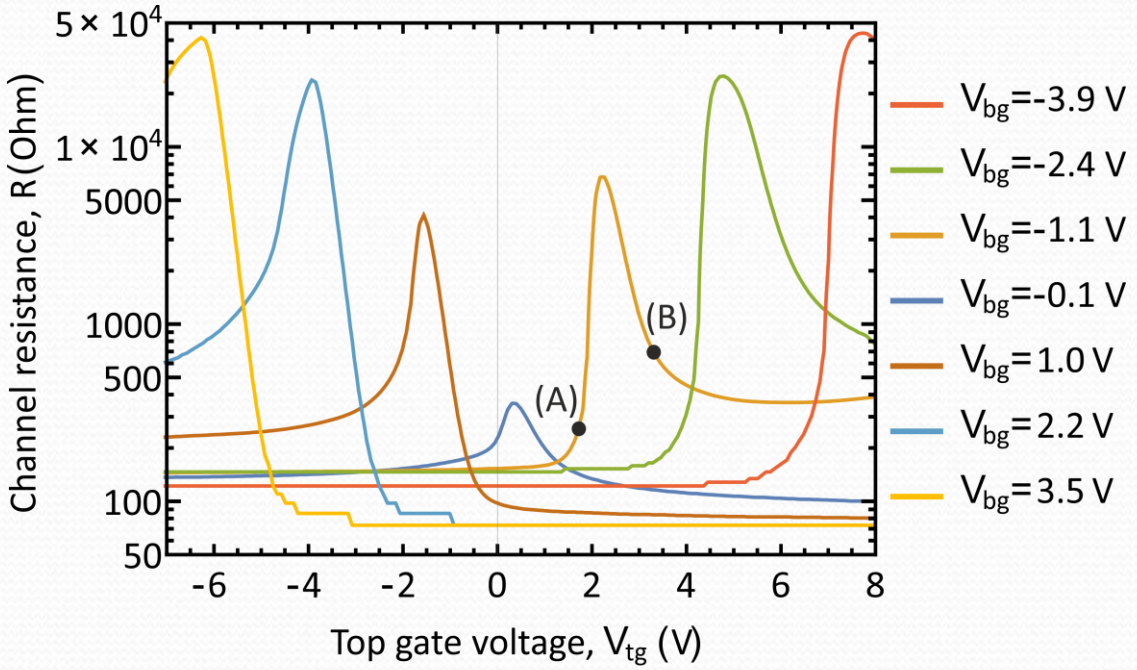
Calculated room-temperature gate transfer (left) and current-voltage (right) characteristics of graphene bilayer TFET at fixed bias voltages at auxiliary gates: V_B = 3.3 V, U_S = −0.6 V, U_D = 0.25 V. Top gate dielectric is 2 nm ZrO_2, κ = 25, back gate dielectric is 10 nm SiO2, spacing between the source doping and control gates d_g = 5 nm, spacing between drain doping and control gates is 10 nm. The regions highlighted in yellow correspond to the drive voltage swing of 150 mV, in which sufficient ON/OFF ratio and high ON-state current are achieved. Inset: gate transfer characteristic in the log scale.

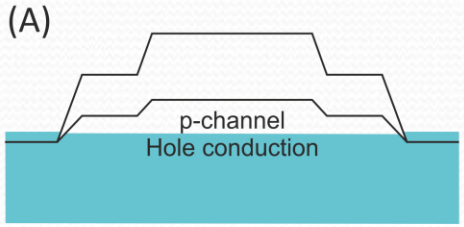
Proposed FET positioning

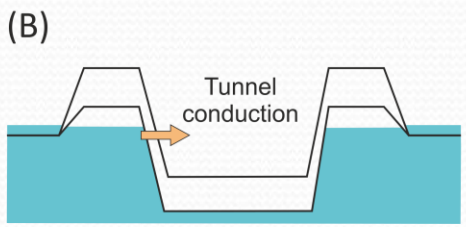


Observation of interband tunneling in GBL









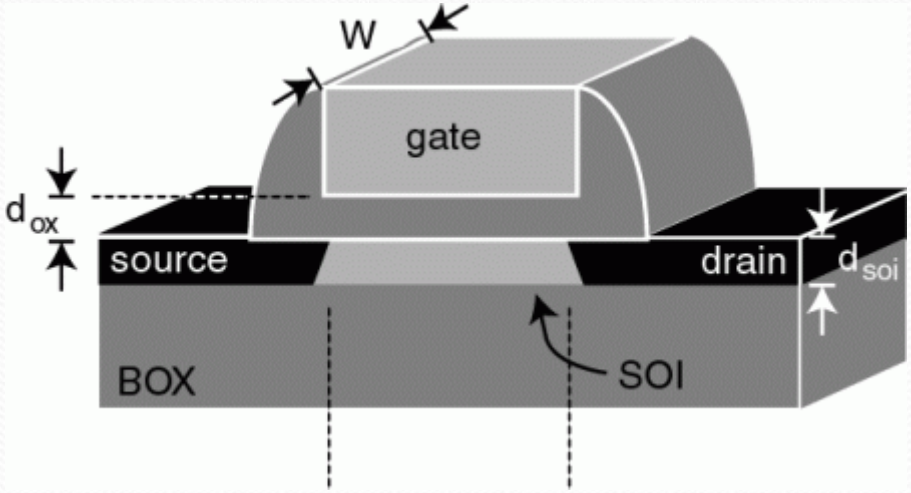
D. A. Bandurin, D. Svintsov, I. Gayduchenko, S. G. Xu, A. Principi, M. Moskotin, I. Tretyakov, D. Yagodkin, S. Zhukov, T. Taniguchi, K. Watanabe, I. V. Grigorieva, M. Polini, G. Goltsman,A. K. Geim, G. Fedorov "*Resonant Terahertz Detection Using Graphene Plasmons*" *Nature Communications* **9**, article number 5392 (2018)

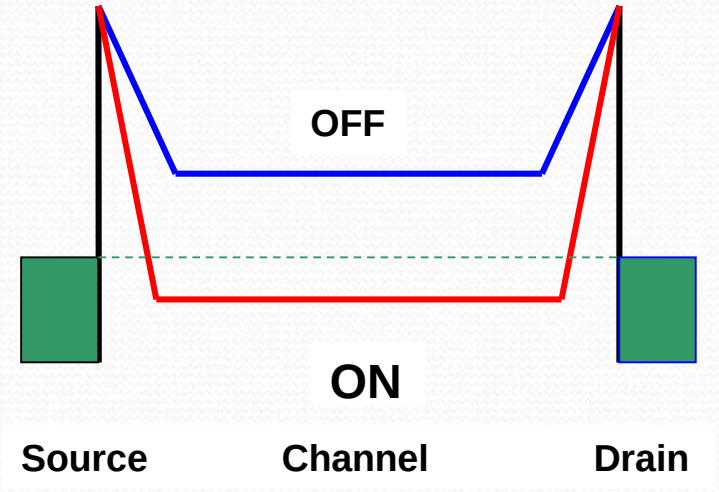
СПАСИБО

За ВНИМАНИЕ!!!


THANK YOU !!!
THANK YOU !!!

Tunnel Schottky Barrier FET: no doping at all





ФТИАН